A DESIGN OF CMOS DIFFERENTIAL VOLTAGE CURRENT CONVEYOR

Kobchai Dejhan, Montree Kumngern, Pipat Prommee and Chatcharin Soonyeekan*

Faculty of Engineering and Research Center of Communication and Information Technology
King Mongkut’s Institute of Technology Ladkrabang, Ladkrabang, Bangkok 10520, Thailand
Email: kobchai@telecom.kmitl.ac.th
Tel: 66-2326-4238, 66-2326-4242, Fax: 66-2326-4554
* Aeronautical Radio of Thailand, 102 Ngamduplee, Tungmahamek, Bangkok 10120, Thailand.

Abstract: A CMOS differential voltage current conveyor is presented. This proposed circuit has a high input dynamic range with high linearity. The input of this proposed circuit is source degeneration differential pair circuit. Its supply voltage is ±1.5 volts; the output of the circuit is class AB. The input dynamic range is ±0.4 volt with -50 dB total harmonic distortion.

1. INTRODUCTION

The differential voltage current conveyor (DVCC) is widely used in analog signal processing circuit such as analog multiplier circuit, squaring circuit, square root circuit, filter circuit [1-3] and etc. DVCC circuit increases the ability of the second generation current conveyor (CCII) [4] by using the input acts as the differential voltage. This differential voltage is widely used for applying in the instrumentation amplifier uses two CCII’s and resistor to connect together as network in order to have the input of CCII as floating instrumentation amplifier, but the error comes from the resistance at node X of CCII (as shown in Fig. 1) is not equal to zero. A DVCC circuit is substituted to overcome this problem and the input dynamic range is greater than CCII. Thus, the signal-to-noise ratio of the circuit is better than the previous design. The proposed circuit of DVCC uses the differential pair input [1-3] by converting the voltage to be the current or so called transconductance circuit with narrow linear input dynamic range. The input dynamic range improvement of DVCC circuit is wide and can be done by extending the linearity of the circuit. The source degeneration is used to increase the linearity of the transconductance circuit [5-6] as shown in Fig. 2.

![Fig. 2 Source generation differential pair circuit](image)

Fig. 2 Source generation differential pair circuit

Therefore, this paper proposes a design of second generation current conveyor with differential input voltage (DVCC), the proposed DVCC has the characteristic as follows; source degeneration differential pair structure, wide input dynamic range, high linearity, low power supply, low power consumption the proposed DVCC uses ±1.5 volts supply voltage, the output signal is class AB in order to save the power consumption.

![Fig. 1 DVCC block](image)

Fig. 1 DVCC block

Let the transistors M1 and M2, M3 and M4 as shown in Fig. 2 are matching, the transistors M1 and M2 operate in saturation region but the transistors M3 and M4 operate in triode region. Therefore, the transfer characteristic of the transconductance is as follow: [5]
\( i_o = \sqrt{\frac{2K_i I_o}{1 + \frac{K_i}{4K_s}} v_i} \)

\[ (2) \]

Where \( v_i = v_{i1} - v_{i2} \), and \( K_i \) is the transconductance of MOS transistor \( M_i \). It is obviously shown that the non-linear term is in the square root and can be neglected; its value is less than one, then the linearity and the input dynamic range can be assigned. It should be noted that the increasing of non-linearity will effect the decreasing of frequency bandwidth.

**2. CIRCUIT DESCRIPTION**

The source generation differential pair circuit as shown in Fig. 2 is used to implement the proposed DVCC circuit. It is implemented as transconductor circuit with high linearity and acts as the input of DVCC circuit. Two sets of the source generation differential pair circuit are needed; it means the transistors M1 to M11. The transistors M1 to M4 are two sets of differential pair; they operate as input of DVCC circuit. The transistors M5 to M6 are active load, the transistors M6 to M11 supply the current, for \( I_z \) is the reference current. The transistors M1 to M4 operate in saturation region, thus the drain current is able to express as in Eq. (3).

\[ I_D = \mu C_{ox} \left( \frac{W}{2L} \right) (V_{gs} - V_T)^2 \]  

\[ (3) \]

Where \( \mu \) = carrier mobility 
\( C_{ox} \) = gate capacitance per unit area

Then, the relation of the four drain currents is as follows.

\[ I_{D,M1} - I_{D,M3} = I_{D,M4} - I_{D,M2} \]  

\[ (4) \]

and get

\[ V_{G,M1} - V_{G,M3} = V_{G,M4} - V_{G,M2} \]  

\[ (5) \]

But \( V_{G,M1} = V_{i1}, V_{G,M3} = 0, V_{G,M4} = V_x \) and \( V_{G,M2} = V_z \). The relation of three-terminal pair can be written as follow;

\[ V_x = V_{i1} - V_{i2} \]  

\[ (6) \]

The output signal of the proposed circuit uses the class AB for saving the energy. The transistor M15 is used for signal level shifting and operates with the transistors M12 and M14. The current source \( I_{B1} \) is used to bias the transistor M16, normally the current passes the transistors M16 and M17 is about 15 \( \mu \)A which is equal to the current passing the transistors M18 to M24. While there is the input signal at terminal X, the transistors M16 and M17 will alternatively operate at each cycle of the signal, such as \( (V_{i1} - V_{i2}) > 0 \) and the resistor; \( R_X \) is connected with the terminal X.

The signal current at terminal X is expressed as

\[ i_X = \frac{V_{i1} - V_{i2}}{R_X} \]  

\[ (7) \]

Thus, the relation can be obtained that \( I_{D,M17} = I_{D,M16} + i_X \) while the transistors M19 and M20 are connected as current mirror from the transistors M16 and M17. Then, \( I_{D,M3} = I_{D,M1} + i_X \) is equal to \( I_{D,M17} = I_{D,M16} + i_X \) for \( I_{D,M19} \) and \( I_{D,M20} \) are the biasing current which reflect from \( I_{D,M16} \) and \( I_{D,M17} \). The output current \( i_{Z2} \) is equal to \( i_X \) flowing in the same direction or \( i_{Z1} = i_Y \). The transistors M20 and M21 are connected as current mirror which reflect the current from M16 and M17. The transistors M20 and M23 are cross connected, the drain current of M20 is used as the reference current for transistor M22, and the drain current of transistor M21 is used as the reference current for transistor M23. Therefore, at terminal X and terminal Z2, there are the flowing currents in opposite direction it means \( i_{Z2} = -i_X \). At the terminals \( Z_1 \) and \( Z_2 \), there are the signals in opposite direction. The characteristics of the proposed DVCC circuit (as shown in Eq. (1)) can be described, the resistance at various terminals can be analyzed by using as small signal circuit.

The resistances at terminals \( X(z_1), Z_1(z_2) \) and \( Z_2(z_2) \) can be carried out as following equations.

\[ r_X = \frac{V_{i1}}{i_X} \]  

\[ (7) \]

\[ r_{Z1} = \frac{1}{g_{ds18} + g_{ds19}} \]  

\[ (8) \]

\[ r_{Z2} = \frac{1}{g_{ds24} + g_{ds25}} \]  

\[ (9) \]

It should be noted that the resistance at terminal Y or Y(\( r_y \)) is very high value (\( \approx \infty \)) because the resistance at gate terminal of MOS transistor is quite high.

\( g_m \) : transconductance of MOS transistor.

\( g_{ds} \) : drain-to-source transconductance

Let \( g_{m3} = g_{m6} = g_{m16} = 197 \mu \)S, \( g_{m17} = 120 \mu \)S, \( g_{ds18} = 6.61 \)nS and \( g_{ds19} = 8.87 \)nS, [6] thus, the resistance at \( X(z_1) = 0.8 \) \( \Omega \), the resistance at \( Z_1(z_2) = 64 \) M\( \Omega \) and the resistance \( Z_2(z_2) = 64 \) M\( \Omega \).

**3. RESULT**

All results are carried out based on simulation with PSpice program simulator by using the parameters of 0.5 \( \mu \)m CMOS technology with level 3 [6]. The W/L ratios of transistors are shown in Table 1.
Fig. 3 Proposed DVCC circuit

Fig. 4 Output current of class AB

Fig. 5 Relation between $I_X$ and $V_{Y1}$, $V_{Y2}$

Fig. 6 Relation between $I_{Z1}$, $I_{Z2}$ and $V_{Y1}$, $V_{Y2}$

Fig. 7 Frequency response of $I_Z/I_X$

Fig. 4 shows the output current of class AB of the proposed circuit by injecting the current at the terminal X. The flowing current in the transistors M16 and M17 are observed, as the transistors M16 and M17 alternatively operate.

Fig. 5 shows the relation of $I_X$ and $V_{Y1}$, $V_{Y2}$ by connecting the 20 kΩ resistance at terminal X, and supply the voltage at terminals $Y_1$ and $Y_2$. The voltage $V_{Y2}$ increases 0.1 volt for each step, then the measurement of the flowing current across 20 kΩ resistance which is connected at terminal X in order to measure the input dynamic range of the proposed circuit. The input dynamic range is ±0.4 volt.

Fig. 6 shows the relation between $I_{Z1}$, $I_{Z2}$ and $V_{Y1}$, $V_{Y2}$ while the terminals $Z_1$ and $Z_2$ are connected with 20 kΩ resistance.

Table 1 W/L of MOS transistors

<table>
<thead>
<tr>
<th>MOS transistor</th>
<th>W/L (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2, M3, M4</td>
<td>20/2</td>
</tr>
<tr>
<td>M5, M6</td>
<td>80/2</td>
</tr>
<tr>
<td>M7, M8, M9, M10, M11</td>
<td>15/2</td>
</tr>
<tr>
<td>M12, M14, M15</td>
<td>4/2</td>
</tr>
<tr>
<td>M13</td>
<td>16/2</td>
</tr>
<tr>
<td>M16, M18, M20, M22, M24</td>
<td>10/2</td>
</tr>
<tr>
<td>M17, M19, M21, M23, M25</td>
<td>40/2</td>
</tr>
<tr>
<td>MS1, MS2, MS3, MS4</td>
<td>4/4</td>
</tr>
</tbody>
</table>

Table 1 W/L of MOS transistors
The frequency response of \( (V_{r2} - V_{r1})/V_X \) is shown in Fig. 8, but the frequency response of \( (I_Z/I_X) \) is shown in Fig. 7. Both frequency responses are quite wide for -3dB down; they are about 80 MHz and 90 MHz, respectively.

The linearity test has been also carried out by applying the 1 MHz signal with various amplitudes at terminal Y and the signal at terminal X are measured from signal simulation. The 0.8 V\(_{pp}\) signal amplitude will have the total harmonic distortion (THD) about -50 dB. Figs. 10 and 11 are the simulation results for carrying out the resistances at terminals X and Z and the resistances at terminals X and Z are 1.72 Ω and 60 MΩ, respectively.

4. CONCLUSION

The paper proposes a type of CMOS differential voltage current conveyor based on CMOS technology. The proposed circuit has good performance, ±0.4 Volt input dynamic range, high linearity, voltage mode, ±1.5 volt supply voltage, class AB output, as shown in Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.5 µm</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>±1.5 Volt</td>
</tr>
<tr>
<td>Input dynamic range</td>
<td>±0.4 Volt</td>
</tr>
<tr>
<td>THD@1MHz: 0.8 V(_{pp})</td>
<td>-50dB</td>
</tr>
<tr>
<td>( R_X )</td>
<td>1.72 Ω</td>
</tr>
<tr>
<td>Power consumption</td>
<td>670 µW</td>
</tr>
</tbody>
</table>

REFERENCES