Fully-Differential High-order Low-pass Filter based on Cascode OTA

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Abstract— This paper presents a design of fully-differential high-order low-pass filter based on cascode OTA. Due to the high-order ladder filter has low sensitivity and suitable for high performance filtering the desired signal. The fifth-order RLC ladder is used as the prototype and the signal flow graph (SFG) is used as the synthesis technique. The cascade OTA is used as the active building blocks. Full-differential scheme is constructed for obtaining the several advantages as well as wide bandwidth and noise minimization. The completed filter circuit consists of 10 OTAs, 10 grounded capacitors based on ±1V power supplies. Frequency response of proposed filter can be tuned between 300kHz and 20MHz through 1 µA to 400 µA of OTA bias currents. Low THD can be achieved as low as 0.15% at 10MHz frequency range.

I. INTRODUCTION

The analog communications signal processing is well known that needs several functions for obtaining the desired signal and removing the unwanted signals. Analog filter is an important subsystem for achieving their functions. First of all, RLC [1] circuits are preferred to use as a filter in the system but they had drawbacks if the band of frequency was changed. Manually tuned of capacitors and inductors was required but it is not practically used. Next generation of electronic design using large scale integrated circuit (LSI) was exhibited. Versatile amplifier named OPAMP and RC [2-4] were preferred to design as well as analog filter. Although, the manual tunability can be done but the completed system is quite large and cannot provided electronically controlled feature. In modern communication signal processing, several building block are integrated as monolithic single chip. The function of several blocks need programmable, small die area and low power supply. Several active building blocks such as OTA [5], CCII [6] and CDTA [7] are introduced for biquad filters. Unfortunately, the performance of biquad filter is quite limited due to the second-order function behaviors. In many cases, the analog signal processing needs the accurate and high performance filter. High-order filter is a solution to be obtained the output requirement. Due to low sensitivity requirement, cascade structure of second order is not suitable to obtain the high-order filter. RLC ladder filter is also called Cauer network is preferred to use as a prototype because it has low-sensitivity feature. Several active devices can be realized using RLC ladder simulation method. OPAMP [1] with RC was implemented but not suitable for integration. Current-mode method based on different active devices is also introduced but some of them suffered from floating passive elements and some circuits used resistors. In the CMOS IC design, resistors can be realized by layout of polysilicon length which inverse proportional with the resistance value. So the large die area is required if the resistors are used. Another drawback is the use of floating capacitor which is not preferred for integrated circuit due to the very serious problem of bottom plate and the substrate [8]. The benefit of differential structure is proved that suitable for high-frequency, second harmonic cancellation and low-noise analog signal processing [9].

This paper presents a fifth-order low-pass filter using fully-differential structure based on CMOS cascode OTA. Signal flow graph (SFG) is used as synthesis method from Chebyshev RLC prototype. OTA-based fully-differential lossy and lossless integrators are realized by cascode OTA and grounded capacitors. Based on the configuration, the results confirmed that the high-frequency operation with low-THD can be achieved. The frequency response of proposed filter can be controlled by adjusting the OTA bias current. Moreover, low-complexity and low-power consumption are also achieved.

II. ACTIVE BUILDING BLOCKS

A. Fully-differential Cascode OTA

All subsystems of proposed filter are realized by cascode OTA [9]. This OTA consists of 2 NMOS and 2 PMOS transistors and 2 current sources which performed as a fundamental active building block as shown in Fig.1.

![Fig. 1 CMOS fully-differential cascode OTA](image)

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![Fig. 2 Symbol of fully-differential cascode OTA](image)

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The electrical symbol and its property of cascode OTA have one of high-impedance of differential voltage input and one of differential output current which are depicted in Fig.2. Assuming that all transistors are operated in the saturation region and the substrates of these transistors are connected to their respective sources. The transconductance can be expressed as

\[ G_m = \pm \frac{g_m g_{m2}}{g_{m1} + g_{m2}} + \frac{g_m g_{m4}}{g_{m3} + g_{m4}} \]  

(1)

where \( g_m = \sqrt{\mu C_{ox} (W/L) I_B} \) with \( I_B \) is an external DC bias current of this element, \( \mu \), \( C_{ox} \), \( W \) and \( L \) are surface mobility, oxide capacitance, channel width and length of MOS transistors \( i \), respectively. Note that the transconductance in Eq.(1) can be tuned by adjusting the bias current.

B. Current-mode Fully-differential Integrators

The integrator circuit is an essential building block in the analog signal processing area. Two types of integrator can be classified by different magnitude and phase responses named as lossy and lossless integrators. Firstly, fully-differential lossless integrator comprises a differential output OTA and two grounded capacitors which depicted in Fig.3 and its transfer function is expressed as

\[ \frac{I_O}{I_{IN}} = \pm \frac{g_m}{sC} \]  

(2)

\[ +I_N \quad -I_N \]
\[ +I_O \quad -I_O \]
\[ +g_m \quad +g_m \]
\[ +2C \quad +2C \]
\[ -\]
\[ + \]
\[ \text{Fig. 3 Fully-differential lossless integrator} \]

Secondly, fully-differential lossy integrator comprises two differential output OTAs and two grounded capacitors which depicted in Fig.4 and its transfer function is expressed as

\[ \frac{I_O}{I_{IN}} = \pm \frac{g_m}{sC + g_m} \]  

(3)

\[ +I_N \quad -I_N \]
\[ +I_O \quad -I_O \]
\[ +g_m \quad +g_m \]
\[ +2C \quad +2C \]
\[ -\]
\[ + \]
\[ \text{Fig. 4 Fully-differential lossy integrator} \]

III. OTA-BASED LADDER FILTER SYNTHESIS

As mentioned that of RLC ladder filter has good resulting in low-sensitivity, the RLC ladder filter is used as a prototype. The simulating passive network by using signal flow graph (SFG) technique and frequency scaling are used for synthesis the active filter. Fifth-order RLC low-pass prototype is shown in Fig.5 and its voltage and current relationships are expressed in Eq.(4)-(12).

\[ V_I = \left( \frac{V_{IN}}{R_f} - I \right) \frac{1}{sC_1}. \]  

(4)

\[ V_I = I \frac{1}{sC_1}. \]  

(5)

\[ V_I = \left( I - \frac{V_{IN}}{R_f} \right) \frac{1}{sC_1}. \]  

(6)

\[ I = I_{IN} - I_z. \]  

(7)

\[ I_z = \frac{V_I - V_{IN}}{sC_2}. \]  

(8)

\[ I_z = I_z - I_z. \]  

(9)

\[ I_z = \frac{V_I - V_{IN}}{sC_2}. \]  

(10)

\[ I_z = I_z - I_z. \]  

(11)

\[ I_z = \frac{V_I - V_{IN}}{sC_2}. \]  

(12)
Considering Fig.7, the old values of $L$ and $C$ have been scaling by the same value ($g_{m}$). The new values of $L$ and $C$ become

$$L_n = \frac{L}{g_{m}} \quad (13)$$

$$C_n = \frac{C}{g_{m}} \quad (14)$$

From Fig.7, it can be seen that $L$ and $C$ components are transformed to lossless and lossy integrator forms. It means that $L_2$ and $L_4$ are replaced by $C_2$ and $C_4$, respectively. The proposed fifth-order ladder low-pass filter can be realized by using block diagram of lossless and lossy integrators and written as Fig.8.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W(μm)</th>
<th>L(μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2</td>
<td>3.6</td>
<td>0.54</td>
</tr>
<tr>
<td>M3, M4</td>
<td>9</td>
<td>0.54</td>
</tr>
</tbody>
</table>

### IV. Simulation Results

The performance of proposed fifth-order current-mode ladder LPF using cascode OTA is verified by PSSpice based on TSMC 0.18µm CMOS Level 7 technology with ±1V power supplies. Transistor aspect ratios of cascode OTA are listed in Table 1.

The operation of lossless and lossy integrators is confirmed by connecting grounded capacitor 10pF and varied bias current from 1µA-400µA. Magnitude and phase response of lossless and lossy integrators are illustrated in Fig.9 and 10, respectively. It can be seen that the frequency response of integrators are varied around 200KHz to 20MHz. Phase response of lossless and lossy integrators is obtained around -90 degrees and -45 degrees, respectively.

The RLC ladder prototype used in this paper is based on Chebyshev function with the following conditions, $f_c$=10MHz, passband ripple=0.5dB, then the passive element values of the RLC prototype can be obtained as $R_R=R_L=1$Ω, $C_1$=28.76mF, $L_2$=L_4=20.73mH and $C_4$=42.83mF. Using the similar concept the passive element of proposed filter are following values, $C_1$=C_3 =14.4pF, $C_2$=C_4 =10.4pF, $C_3$=21.4 nF and bias current of OTAs are given by $I_B$=50µA. The frequency response of RLC prototype and proposed filter are plotted in Fig. 11. It can be seen that the magnitude response proposed filter is in accordance with the RLC prototype.
The tunability feature of proposed filter can be verified by adjusting the bias current from 1μA-400μA. The frequency response of proposed filter can be tuned between 500kHz and 20MHz.

A group delays performance of proposed filter can be verified by setting the bias current at 400μA. Group delays is obtained around 30ns and flatten along the passband but the stopband has higher delays of 60ns.

Filtering performance of proposed filter can be verified by applying multi-tone (100kHz, 300kHz, 1MHz, 3MHz, 10MHz, 30MHz and 100MHz) and setting the bias current at 400μA. Multi-tone spectrums can be obtained only in-band frequency according to the theory.

The distortion is verified by THD simulation in passband at 1MHz and 10MHz. The THD is obtained less than 0.12% as shown in Fig.15.

V. CONCLUSIONS

Fully-differential electronically tunable current-mode high-order LPF is realized based on the Chebyshev ladder low-pass filter prototype. Eleven cascode OTAs and 10 grounded capacitors are used for implementing the proposed filter. It enjoys electronic tuning of frequency response between 500kHz and 20MHz through bias current from 1μA to 400μA. The circuit uses ±1V power supplies with low dynamic power consumption (7.92mW) at 400μA bias current. The proposed circuit enjoys low complexity structures, with, low THD less than 0.12%, it is very suitable to realize the proposed filter in communication monolithic chip to use in low-power mobile communication equipment.

REFERENCES