Abstract—This paper presents CMOS-based current mode fifth-order ladder low-pass filter by using lossy and lossless integrators and grounded capacitors without external resistors. The lossy and lossless integrators are realized based on CMOS technology. The proposed circuit contains 27 NMOS transistors and 5 grounded capacitors. The frequency response can be controlled between 10kHz and 100MHz by adjusting bias current between 0.002 µA and 20 µA. This filter uses 1.5V power supply with 0.8 mW power consumption. Due to the filter consists of grounded capacitors without resistance and uses low power supply, it is suitable for integration. PSPICE simulation results are carried out by TSMC 0.18µm technology.

Keywords—Integrator, ladder, low-pass, low-voltage, tunable filter.

I. INTRODUCTION

P RESENTLY, electronic circuits are continuously developed for not only reducing die areas but also increasing their performances. CMOS technology is used in designing and developing many types of analog signal processing circuit including analog filters. There are many methods to realize the analog filters. Low-order synthesis is a famous method to realize the active filters. First-order [1-2] and second-order [3-4] filters were presented with several devices. Unfortunately, the low-order filters have received many drawbacks in their cut-off frequencies. The cut-off frequency of low-order low-pass filter cannot clearly remove the higher side-band frequencies. Some papers described high-order low-pass filters [5-16] and they rapidly developed based on active building blocks. Op-amp [5-8] and OTA [9-13] were selected devices to realize voltage mode fifth-order ladder low-pass filter by using integrators.

It is well-known that the design of current-mode filter has more advantages than voltage-mode because it has higher frequency response, smaller die area and use lower power supply which suitable for integration. Current mode ladder filter by using multiple outputs current conveyer (MOCC) [12] with resistors was presented, but it suffered from a large number of passive devices. OTAs-based ladder filter [13] was presented, but it contained excessive grounded capacitors and can be tuned in only narrow frequency range. OPAMP connected with MOS transistors [14-16] were presented with complex structures which were not appropriate for integration.

Due to the drawbacks of the previous circuits, tunable CMOS-based current mode fifth-order ladder low-pass filter is proposed in this paper. This filter is realized by a lossy integrator, four lossless integrators and five grounded capacitors. The proposed circuit is operated in transistor-level for achieving the benefits, such as, low component count, low-voltage, low-power and wide-range electronic tuning features. The circuit consists of 27 transistors and 5 grounded capacitors which is suitable for integrations. The simulation results are agreed well with the theory.

II. THEORIES AND PRINCIPLES

A. CMOS-based Integrator

Figure1 shows lossy integrator block diagram that has the same outputs which are \( Y_1 \) and \( Y_2 \). The transfer function can be expressed as

\[
\frac{Y_1 - Y_2}{X} = \frac{A}{s + A}.
\]

Lossless integrator can be easily realized by adding inverting gain to the output \( Y_1 \), then feeding back to the input as shown in Fig. 2. From this concept, the non-inverting and inverting lossless integrator transfer functions are obtained at ports \( Z_1 \) and \( Z_2 \), respectively, as

\[
\frac{Z_1}{X} = \frac{A}{s},
\]

\[
\frac{Z_2}{X} = -\frac{A}{s}.
\]

Figure 3 shows the realization of CMOS-based lossy integrator by using the building block in Fig. 1. The circuit has modified and simplified from the original idea [17]. Small signal model of Fig. 3 and its block diagram can be written as Fig. 4. Suppose that all transconductances are identical, then using KCL analysis in Fig. 4; hence the current transfer

\[
\frac{Y_1}{X} = \frac{A}{s + A}.
\]

Fig. 1. Lossy integrator block diagram

\[
\frac{Z_1}{X} = \frac{A}{s + A}.
\]

Fig. 2. Lossless integrator block diagram

\[
\frac{Z_1}{s} = \frac{A}{s + A}.
\]

Fig. 3. CMOS-based lossy integrator block diagram

\[
\frac{Z_2}{s} = -\frac{A}{s}.
\]

Fig. 4. KCL analysis of current transfer
where \( \mu, C_{\text{ox}}, W \) and \( L \) are surface mobility, channel oxide capacitance, channel width and channel length of MOS transistor, respectively. It can be seen that conductance can be tuned by adjusting bias current \( I_{B} \).

### III. Fifth-order Low-pass Filter Synthesis

Fifth-order low-pass filter is realized from the proposed CMOS-based lossless and lossy integrator by using LC ladder filter Chebyshev prototype. Using doubly terminated LC ladder concept in realization, the filter can be written as Fig.7 and its transfer function is depicted in Eq.(10).

\[
\frac{I_o(s)}{I_{in}(s)} = \frac{1}{s^5 + \frac{1}{C_6} + \frac{1}{sC_5} + \frac{1}{s^2C_4} + \frac{1}{s^3C_3} + \frac{1}{s^4C_2} + \frac{1}{s^5C_1}}
\]

(10)

Considering current and voltage of the fifth-order ladder low-pass filter in Fig.7, their relationship by using KCL analysis can be written as

\[
V_1 = \left( I_{in} - \frac{V_2}{R_1} - I_2 \right) \frac{1}{sC_1}.
\]

(11)

\[
V_2 = \frac{I_3}{sC_2}.
\]

(12)

\[
V_3 = \left( I_2 - \frac{V_1}{R_3} \right) \frac{1}{sC_3}.
\]

(13)

\[
I_4 = \left( I_1 - \frac{V_2}{R_4} \right) \frac{1}{sC_4}.
\]

(14)

\[
I_5 = \left( I_4 - \frac{V_3}{R_5} \right) \frac{1}{sC_5}.
\]

(15)

\[
I_6 = \left( I_5 - \frac{V_4}{R_6} \right) \frac{1}{sC_6}.
\]

(16)

\[
I_7 = \left( I_6 - \frac{V_5}{R_7} \right) \frac{1}{sC_7}.
\]

(17)

\[
I_8 = \left( I_7 - \frac{V_6}{R_8} \right) \frac{1}{sC_8}.
\]

(18)

\[
I_9 = \left( I_8 - \frac{V_7}{R_9} \right) \frac{1}{sC_9}.
\]

(19)

Signal flow graph (SFG) can be written from equations (11)-(19) in the form of current and voltage variables [5] as Fig.8. Transforming the voltage variables to current variables, the normalized value by using the transconductance \( g_m \) is applied into SFG the Fig.8. The normalized SFG of Fig.8 can
be transformed and rewritten in Fig.9.

The values of $L$ and $C$ have been scaling by the same value ($g_m$). The new values of $L$ and $C$ become

\begin{align}
L_a &= \frac{L}{g_m} \\
C_a &= \frac{C}{g_m}
\end{align}

From Fig.9, it can be seen that $L$ and $C$ components are also transformed to lossless integrator forms. It means that $C_2$ and $C_4$ are replaced into $L_2$ and $L_4$, respectively. Considering Fig.9, the proposed ladder low-pass filter can be implemented by using block diagram of lossless integrator in Fig.6. Proposed fifth-order ladder low-pass filter can be written as Fig.10. Considering the last lossless integrator in Fig.10, it has negative feedback to its input; then it performs as lossy integrator. Due to lossy integrator consists of only three transistors, the last lossless integrator can be minimized and rewritten to Fig.11 for achieving smaller circuit die area. Note that, the outputs of lossy integrator are only negative, then the output of low-pass filter is also inverted; but it has no effects to the magnitude responses of the circuit.

IV. SIMULATION RESULTS

In this section, it describes the simulation results of CMOS-based integrators and fifth-order ladder low-pass filter. PSPICE simulation results are carried out by using TSMC 0.18μm CMOS technology [18], +1.5V power supply and all NMOS in Fig.3 and 5 have W/L = 5μm/0.5μm.

The magnitude responses of CMOS-based lossy integrator in Fig.3 and CMOS-based lossless integrator in Fig.5 are shown in Fig. 12 and 13, respectively. Setting capacitor $C_1=0.6pF$, then varying $I_B [0.002, 0.02, 0.2, 2, 20] \mu A$. The transconductance is obtained around $[0.075, 0.75, 7.5, 56.5, 377] \mu S$. The frequency responses can be tuned in a wide range from 10 kHz to 100MHz.

In the design of fifth-order ladder low-pass filter by using RLC Chebyshev prototype with 1dB ripple [19], CMOS-based integrators use capacitors $C_1-C_6$ which are 0.3 pF, 0.6pF, 0.9pF, 0.6pF and 0.3pF, respectively [19]. The current outputs of proposed CMOS-based fifth-order ladder low-pass
filter in Fig. 11 are shown in Fig. 14 by varying $I_B$ [0.002, 0.02, 0.2, 2, 20] μA. The frequency can be tuned in a wide range from 10 kHz to 100MHz. The magnitude response between the prototype ladder function in Eq.(10) with scaling the components (10 times scaling per decade) by Eqs.(20) and (21) and proposed filter is also compared. It can be seen that the result of proposed filter is in agreement with the theoretical expectation. The error of frequency response is found at high-frequency.

Input impedance of the proposed CMOS-based fifth-order ladder low-pass filter by setting $I_B=20μA$ can be obtained around 1.3kΩ as shown in Fig. 15. Another result of proposed filter can be verified by the filtering performance. Suppose that the cutoff frequency 100MHz ($I_B=20μA$) is defined and two-tone sinusoidal signals with different frequencies of 90MHz and 200MHz are applied at input. The output signal of proposed filter can be obtained only 90MHz as shown in Fig. 16. The signal frequency 300MHz is perfectly removed based on -100dB/decade of proposed LP filter.

Total harmonic distortions (THDs) of the proposed CMOS-based fifth-order ladder low-pass filter are obtained by setting $I_B=20μA$ and applying the sinusoidal inputs 1MHz and 10MHz with varying amplitude of the inputs. Fig. 17 exhibits the THD of 20μA sinusoidal inputs at 1MHz and 10MHz which is lower than 0.3% and 2.2%, respectively.

The comparison of proposed fifth-order LPF with previous works is depicted in Table I. It is shown that the previous works used at least 7 MOOTAs [11], [15] with narrow tunable frequency range. Although another work requires 5 current conveyors [14] without the electronic tunability feature. Note that, at least more than 10 transistors are required for realizing the MOOTA and MOCC. It can be seen that low number of active components (27 NMOS transistors) is achieved in implementing the proposed filter. High-frequency operation and wide range electronic tuning is obtained.

V. CONCLUSION

A novel CMOS-based current mode fifth-order ladder low-pass filter is presented. The circuit is realized from CMOS-based integrators by using the concept of Chebyshev ladder filter prototype. The frequency response can be electronically controlled between 10kHz and 100MHz by adjusting the bias current between 0.002 μA and 20 μA. This circuit uses 1.5V power supply and consumes the power around 0.8mW at 20 μA bias currents. The proposed circuit contains 27 NMOS transistors and 5 grounded capacitors. This circuit provides many attractive features, for examples, low THD, low input impedance, low power supply and wide range frequency controllable.

REFERENCES
