Floating-Capacitance Multiplier based on CCDDCCs and its Application

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Abstract—This paper proposes a new floating capacitance multiplier using three Current Control Differential Difference Current Conveyors (CCDDCCs) with CMOS technology and one grounded capacitor. The circuit can be electronically tuned through bias currents of CCDDCC without external resistor connections and temperature effects do not affect to the capacitance characteristic. The realization is suitable for further integration. The third-order elliptic LPF is included as an application. The simulations results of proposed capacitance multiplier and its applications are carried out by PSpice that agrees well with the theoretical expectations.

Keywords: Floating Capacitance Multiplier, Electronically Tuned, CCDDCC

I. INTRODUCTION

Second-generation current conveyors (CCIIs) [1] proved to be a versatile building block that can be used to implement many analog signal processing circuits such as active filters [2–4], sinusoidal oscillators [5] based on grounded capacitors and resistors. CCIIs have low impedance at X-terminal and high output impedance at the Z-terminal. However, they have lack of the electronic control and require resistor connections. Current-controlled current conveyor (CCCCI) is a more versatile building block that can be electronically controlled the parasitic resistance of X-terminal. It can be realized by BJT [6] and CMOS [7] technologies. The resistorless and electronic tunability of analog signal processing designs have been realized based on CCCI. Differential difference current conveyor (DDCC) [8] and differential voltage current conveyor (DVCC) [9] were discovered and realized for filters [10–17] and oscillator [18]. The accurate performance and high bandwidth are discovered and realized for filters [10–17] and oscillator [18]. Nevertheless, in those circuits used external resistor [1–5], [8–18] which can not be provided electronic tunabilities.

In this paper, a new device CMOS current-controlled differential current conveyors (CCDDCCs) and its application to a floating capacitance multiplier employing three CCDDCCs and one grounded capacitor is presented. The intrinsic resistance at X-terminal can be electronically tuned through the bias current of CCDDCC without using external resistors connections. In the application, elliptic low-pass filter is raised to confirm the theoretical expectation. The proposed circuit is suitable for IC production.

II. GENERAL PRINCIPLE

A. CMOS Differential Voltage Buffer

The CMOS differential voltage buffer (DVB) as shown in Fig.1. The circuit structure of this CMOS DVB is similar to the DDA realizations in [19]. The input transconductance elements are realized with two differential stages (M1 and M2; M3 and M4). The high-gain stage is composed of a current mirror (M5 and M6). It converts the differential current to a single-ended output current (M7). The output voltage of this amplifier can be expressed as

\[ V_y = V_{y1} - \beta_{y1} V_{y2} + V_{y3} \]  \hspace{1cm} (1)

In the discussion so far, we have assumed that the current mirror has unity gain, and transistors are perfectly matched. However, in practical realizations, several non-idealities must be presented. The major factors will be considered are the finite transconductance (g) of the transistors, and transistors mismatched. The relationship among \( V_{y1}, V_{y2}, V_{y3}, \) and \( V_y \) can be obtained using small-signal analysis. The transistors in Fig.2 are replaced by appropriate equivalent circuits and the node equations can be derived. To simplify discussion, the body effect has been neglected and the two differential pairs are assumed to be identical. Then, by solving the equations, we obtain

\[ V_x \approx \beta_{y1} V_{y1} - \beta_{y2} V_{y2} + \beta_{y3} V_{y3} \]  \hspace{1cm} (2.1)

\[ \beta_{y1} \approx \frac{g_{m1} g_{m2}(g_{m4} + g_{m5} + g_{m6})}{g_{m2}g_{m3} + g_{m5}g_{m4} + g_{m6}g_{m7}} \]  \hspace{1cm} (2.2)
\[
\beta_1 = \frac{-g_{d1}g_{m1}g_{m2}}{g_{d1}g_{m1}g_{m2} + g_{d1}g_{m2} + g_{d2}g_{m2} + g_{d1}g_{m1} + g_{d2}g_{m1} + g_{d2}g_{m1}} \\
\beta_2 = \frac{g_{m1}g_{m2}}{g_{d1}g_{m1}g_{m2} + g_{d1}g_{m2} + g_{d2}g_{m2} + g_{d1}g_{m1} + g_{d2}g_{m1} + g_{d2}g_{m1}} \\
\beta_3 = \frac{g_{m1}g_{m2}}{g_{d1}g_{m1}g_{m2} + g_{d1}g_{m2} + g_{d2}g_{m2} + g_{d1}g_{m1} + g_{d2}g_{m1} + g_{d2}g_{m1}}
\]

(2.3) \hspace{1cm} (2.4)

Where, \( g_{d1} \) and \( g_{m1} \) denote the drain conductance and transconductance of transistor \( M_1 \), respectively. There are clear that the voltages at \( Y_1 \), \( Y_2 \), and \( Y_3 \) terminals will be accurately transferred to \( X' \)-terminal if and only if \( g_{m1} \approx g_{d1} \).

Similarly, the terminal impedance looking into \( X' \)-terminal can be derived by setting \( V_{Y1} \), \( V_{Y2} \) and \( V_{Y3} \) to zero, applying a test voltage \( V_X \) at node \( X' \), and calculating the current \( I_X \). It is evident that the \( X' \)-terminal resistance will be very low if and only if \( g_{m1} \approx g_{d1} \). This result

\[
r_f = \frac{g_{m1}g_{m2}}{g_{d1} + g_{d2} + g_{m1}}
\]

(3)

B. Current-controlled Current Conveyor (CCCI)

A CCCI is a versatile active building block including 3-terminals, \( X \), \( Y \) and \( Z \). The relationship between voltage and current variables at \( X \), \( Y \) and \( Z \) terminals of ideal CCCI can be described as \( i_x = 0 \), \( \varepsilon_{xy} = \varepsilon_{x'z} \) and \( i_{x'} = i_z \). Where the positive and negative signs of the current \( i_z \) denoted the positive (CCCI+) and negative (CCCI-), respectively, and \( R_X \) is an intrinsic resistance of CCCI. The circuit configuration of conventional CMOS CCCI is illustrated in Fig.2 based on complementary source follower [7]. The \( X \)-terminal impedance is calculated by

\[
R_X = \frac{1}{\sqrt{8\mu pC_{ox} W/L} I_Z}
\]

(4)

Whereas, \( \mu \), \( C_{ox} \), \( W \) and \( L \) are, respectively, surface mobility, oxide capacitance, channel width and length of MOS transistors \( (M_{19} \) and \( M_{20} \)). Consequently, \( R_X \) can be tuned electronically by current bias \( I_B \).

![Fig.2 CMOS CCCI circuit](image)

The relationship between \( V_Y \) and \( V_X \) without load connected at \( X \)-terminal can be obtained by using small-signal analysis. The transistors in Fig.3 are replaced by equivalent circuits and the node equations can be derived. Then, by solving the equations, we obtain

\[
\frac{V_X}{V_Y} = \beta_1 = A + B
\]

(5)

Where, \( A \approx g_{m1}g_{m2} (g_{d1} + g_{d20}) + g_{m1}g_{m19} (g_{d10} + g_{d21}) \), and \( B \approx g_{m1}g_{m2} (g_{d10} + g_{d21}) \).

C. Basic Concept of CMOS CCDDCC

The CCDDCC properties are similar to the conventional DDCC or DVCC, except that resistance at \( X \)-terminal of CCDDCC has finite input resistances \( R_X \). This intrinsic resistance \( (R_X) \) can be controlled by the bias current \( I_B \) as shown in Eq.(1). The symbol and the equivalent circuit of the CCDDCC are illustrated in Fig.3 (a) and (b), respectively.

![Fig.3 CCDDCC circuit (a) Symbol (b) Equivalent circuit](image)

D. Current Controlled Differential Difference Current Conveyor (CCDDCC)

The internal realization of CCDDCC is done by connecting \( X' \)-terminal of DVB with \( Y \)-terminal of CCCI which as shown in Fig.4. Due to the low-output impedance of DVB and high-input impedance of CCCI as discussion in section C, the DVB can cascade connect to CCCI. Voltage gain at \( X \)-terminal with respect to \( Y \)-terminal denoted by \( \beta = \beta_1 + \beta_2 \). Current gain at \( Z \)-terminals from \( X \)-terminal denoted by \( \pm \alpha \). The properties of DCC and CCCI are combined which can be described in the following matrix equations:

\[
\begin{bmatrix}
V_{X} \\
I_{T1} \\
I_{T2} \\
I_{T3} \\
I_{T4}
\end{bmatrix}
= \begin{bmatrix}
R_X & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
\pm 1 & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I_{X} \\
V_{Y} \\
V_{Z} \\
V_{Y1} \\
V_{Y2}
\end{bmatrix}
\]

(7)

![Fig.4 CMOS current-controlled differential difference current conveyor (CCDDCC)](image)
the current and voltage relationship as deviation if all CCDDCC are matched. The capacitance has
been simulated by PSpice with power supplies, \( V_{DD} = V_{SS} = 1.25V \) and bias voltage, \( V_B = 0.55V \). Transistor aspect ratios are listed in Table 1 and used TSMC MOSIS 0.25\( \mu \)m model are shown in Table 2.

\[
\frac{V_x}{I_x} = \begin{bmatrix}
R_x & \frac{\alpha_x}{\beta_x} & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I_x
\end{bmatrix}
\tag{8}
\]

\[
I_{x1} = \frac{V_{X1}}{R_{x1}}
\]
\[
I_{x2} = \frac{V_{X2}}{R_{x2}}
\]
\[
I_{x3} = \frac{V_{X3}}{R_{x3}}
\]
\[
\alpha = \frac{\beta}{\beta_2}
\]

From Eq.(9)-(12) X-terminal resistance of CCDDCC3 the X3 is cancelled by value \( R_{X3}=R_{x1} \), so the equation input impedance from Fig.5 as shown in Eq.(13)

\[
Z_{eq} = \frac{V_{in}}{I_{in}} = \frac{R_{x1}}{sR_{x2}C}
\tag{13}
\]

From Eq.(13) capacitor value can be tuned capacitance at X-terminal resistance of the CCDDCC1 and CCDDCC2 which of the \( R_{X1} \) and \( R_{X2} \) respectively and the equivalent capacitance value can be expressed as

\[
C_{eq} = K_{cs} C = \frac{R_{x2}}{R_{x1}}
\tag{14}
\]

where

\[
K_{cs} = \frac{R_{x2}}{R_{x1}} = \frac{I_{B1}}{I_{B2}}
\tag{15}
\]

Consider of non-ideal capacitor, the capacitor value becomes

\[
C_{eq} = K_{cs} C = \frac{\beta}{\beta_2} \frac{\alpha_x R_{x2} C}{\beta_2 R_{x2} R_{x1}}
\tag{16}
\]

From Eq.(16) the capacitance value has slightly deviated if all CCDDCC are matched. The capacitance has also insensitive from the temperature.

### III. Simulation Results

This proposed floating-capacitance multiplier circuit as shown in Fig.5 to verify characteristic and performance are simulated by PSpice with power supplies, \( V_{DD} = V_{SS} = 1.25V \) and bias voltage, \( V_B = 0.55V \). Transistor aspect ratios are listed in Table 1 and used TSMC MOSIS 0.25\( \mu \)m model are shown in Table 2.

<table>
<thead>
<tr>
<th>Transistors</th>
<th>( W(\mu\text{m}) )</th>
<th>( L(\mu\text{m}) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( M_1 - M_2 )</td>
<td>1</td>
<td>0.25</td>
</tr>
<tr>
<td>( M_{X1}, M_{Y1} )</td>
<td>5</td>
<td>0.25</td>
</tr>
<tr>
<td>( M_{X2}, M_{Y2} )</td>
<td>8</td>
<td>0.25</td>
</tr>
<tr>
<td>ALL NMOS</td>
<td>3</td>
<td>0.25</td>
</tr>
<tr>
<td>ALL PMOS</td>
<td>5</td>
<td>0.25</td>
</tr>
</tbody>
</table>

**Table 1 Aspect ratio of transistor for CCDDCCs**

**Table 2 Parameter of transistor model TSMC MOSIS 0.25\( \mu \)m**

**MODEL NMOS, NPMOS TLEV=LEVEL3 TOX=5E-7 NSUB=1E16 GAMMA=0.6348369**

**MODEL PMOS NPMOS TLEV=LEVEL3 TOX=5E-7 NSUB=1E16 GAMMA=0.6348369**

**Fig.6 Input-impedance characteristic while \( I_{in} \) is adjusted**

**Fig.7 Impedance of capacitor while temperature 0-100C is adjusted**

**Fig.8 shows an impedance of proposed floating capacitor circuit. The original capacitor 10pF is used and bias current of CCDDCC1, CCDDCC2 are \( I_{in} = I_{in2} = 10\mu A \). The circuit can be electronically tuned through bias current of CCDDCC2, \( I_{in2} = 0.1\mu A \) to 10\( \mu A \). It is clear that the capacitance can be operated along input frequency range more than 10MHz. The capacitance value can be tuned based on \( I_{in2} \) as discussed in Eq.(15) with 1 to \( \sqrt{10} \) of the multiplication index. The temperature insensitive of capacitance is verified by varying the temperature from 0 to.
to 100 degree Celsius as shown in Fig.7. The temperature has no effects from the temperature as discussed in Eq.(16).

IV. FLOATING-CAPACITANCE MULTIPLIER APPLICATION

The example of the proposed floating capacitance multiplier to confirm the realistic application and theoretical is discussed in this section. The proposed floating capacitance multiplier can be flexibly used in grounded and floating forms. The 3rd order LP elliptic filter prototype [20] as shown in Fig.8 is used to confirm the application.

Using the equaled capacitances and equaled resistances, the voltage transfer function of Fig.8 can be written as

\[ \frac{V_o}{V_s} = \frac{s^2LC + 1}{3s^3LC^2 + 4s^2LC + s(2RC + L/R) + 2} \]

(17)

The current biases are the following conditions, \( I_{B1}=I_{B2}=10 \mu A \), and \( I_{B3} \) is varied from 1\( \mu A \) to 8\( \mu A \). The original capacitor of proposed floating capacitance multiplier circuits is 100\( pF \). The inductor and resistors are assigned to be \( L=10 \mu H \), \( R=1 k\Omega \), respectively. The simulation of tunable 3rd order LP elliptic filter is shown in Fig.9.

V. CONCLUSION

The realization of floating capacitance multiplier employing CMOS-based CCDDCC is presented. The proposed capacitance multiplier provides widely used in either grounded or floating forms. The resistorless, temperature insensitive and electronic tunability are attractive features which suitable for further IC production. The LC prototype can be implemented by using proposed circuit instead to confirm realistic application.

REFERENCES


