Current-mode Multiphase Sinusoidal Oscillator
based on CCCII All-pass Networks

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Abstract—This paper proposes a realization of all-pass networks and multiphase sinusoidal oscillator using loop-back of n-cascaded of all-pass sections. Three Multiple Outputs current-controlled current conveyor (CCCIIs) and a grounded capacitor are constructed as current-mode all-pass networks (APN) with electronic controlled for gain and frequency response. The proposed n-cascaded APNs are constructed with a unity gain loop-back for achieving the multiphase sinusoidal oscillator (MSO). The orthogonally of the oscillate condition and the frequency of oscillation are obtained with their electronic controlled through a particular CCCII current biased. The proposed multiphase sinusoidal current output and the voltage output can be obtained with equally space in phase of 360°/n degree. The third-order oscillator has been raised up to confirm the theoretical agreement. The low-harmonic distortion of the achieved sinusoidal output less than 0.9% is obtained. The simulation results are carried out by PSpice for confirming its characteristics and performances.

Keyword: Oscillator, Multiphase, All-pass, CCCII

I. INTRODUCTION

In recent years, the synthesis of voltage-mode and current-mode sinusoidal oscillators have received considerable attention [1-5] using 2nd order loop-back function. Unity gain is connected with basic passive RC network [1]. Voltage-controlled frequency using OTA was introduced for voltage-mode operations [2]. New designed methods of the oscillator were developed with current-mode for taking their benefits. Current Follower (CF) with RC networks [3] and compensated poles of OPAMP (OA) [4] are recent methods for realizing current-mode oscillator. Also Current-conveyor (CCII) with passive RC was an interesting method for current-mode implementations [5]. All-pass network was also implemented for current-mode quadrature oscillator using CCII [7-11]. Unfortunately, unity gain all-pass network were introduced but they lack of gain adjustment.

Lower-order of filter function is definitely less accurate than higher-order counterpart. High-order oscillators using high-order low-pass filter with loop back function were introduced [12-18] in a few years ago. Multiphase Sinusoidal Oscillator (MSO) is used because MSO provides more sinusoids with poly-phases difference. For example, in telecommunications, MSO is used for phase modulator, quadrature mixers and single-sideband generators. In the measurement purposes, MSO is used for vector generators or selective voltmeters. Many devices can be realized for the oscillators such as CF, OA, CCII, OTA and CFOA (Current Feedback Operational Amplifier). In order to be low complexity construction, OTA is a simple interesting device with also electronically controllable characteristic.

High-order network is formulated to obtain high-purity output. Lossy and lossless integrators were preferred for obtaining the MSO by using n-cascaded structure based on high-order low-pass filter. The first and the second of 3rd order MSO has been introduced by using RC based on different active components, CCII [12] and OA [13] integrator sections. The third MSO has been introduced, based on CCII integrator sections [14] for controlling oscillation frequency electronically. All of three MSOs provide the adjusting of each stage-gain (k)=-2 by resistors and capacitors. Accurate stage-gain can not be obtained which have to be slightly adjusted for achieving the oscillate condition. It is impractical for slightly adjusting of stage-gain by the passive elements [14]. Other MSOs were introduced based on OTA [15] integrator sections with loop-back gain (k)=-8. Although, these achieved circuits were able to electronic-controlled of oscillate condition but they lacked of equally amplitude of each phase which complicated in the applications. All-pass based MSO has been introduced by using OA and RC network [16]. The CDTA with floating capacitor was also formed as LPN [17] and APN-based MSOs [18]. None of equally spaced in phase of each output and floating capacitor are the weak points of this circuit. It is therefore not suitable for IC production especially the CDTA. Low-bandwidth and power consumption are the suspicious problems.

In this paper, CMOS CCCII-based MSO is implemented for either generalized odd/even phase oscillator. The proposed all-pass section is constructed by using 3 CCCIIs and only a grounded capacitor without the resistor connection. Each stage-gain is able to be electronically-controlled through particular CCCII current biased independent with its natural frequency. Generally, oscillator needs to maintain its loop-gain to be unity. Proposed all-pass section with stage-gain adjustment is suitable to oscillator application. The proposed configuration is implemented for equally space in phase MSO and further IC production. For odd phase, we utilize CCCII-based all-pass networks in the negative mode for the phase-shifting network that is incorporated in the feedback loop. High-order feedback loop again results in...
precise oscillating frequencies and low harmonic distortion in a simple circuit.

The proposed MSO structure yields the following features.

1) Low complexity structure, the cascadable of each section can be easily configured to realize using the minimum number of active and passive components per phase;
2) Equally spaced in phase and amplitude of each output.
3) Use of grounded capacitors with no externally connected resistors; this would be attractive for integration;
4) The frequency of oscillation and oscillation condition can be controlled through the devices current biased without disturbance of each other; this would pave the way for electronic tunability;

They are the main intentions of this paper to propose such a MSO structure.

A) Principle of n-cascaded APN-based oscillator

The generalized structure of an n-phase sinusoidal oscillator is shown in Fig.1. It consists of n-cascaded first-order inverting all-pass transfer functions called an all-pass network (APN). The current output (Io) of the nth stage is fed back to the input of the first stage. Each section is determined by the transfer function.

\[
\frac{I_o}{I_x} = -k \frac{1 - sT}{1 + sT} \tag{1}
\]

Where \( k \) denotes the low-frequency stage gain and \( T \) denotes the system time constant which determines the cut-off frequency \( f_0 \). The system loop-gain is given by

\[
H(s) = \left( -k \frac{1 - sT}{1 + sT} \right)^n = 1 \tag{2}
\]

For oscillation at the frequency \( \omega_0 = 2\pi f_0 \), the Barkhausen condition must be satisfied such that

\[
H(j\omega_0) = \left[ -k \left( \frac{1 - j\omega_0 T}{1 + j\omega_0 T} \right) \right]^n = 1 \tag{3}
\]

Which is equivalent to

\[
|H(j\omega_0)| = 1 \tag{4}
\]

Phase equals 360 degrees at the frequency of oscillation. Assumed \( n \)-stages each with phase shift \( \phi \), the total of phase (each stage equals 2 phase difference) \( 2n \) for 1 cycle can be expressed as

\[
\angle H(j\omega_0) = 2n\phi = 2n\left( -2\tan^{-1}\omega_0 T \right) = -2\pi \tag{5}
\]

Whereas \( \phi \) is the phase shift of each all-pass section. It should be noted that Eq.(3) has a solution only if the value of \( n \) is odd \( (n \geq 3) \). From Eq.(5), there are \( n \) outputs \( I_o \) \((i = 1, 2, \ldots, n)\). Each output is shifted in phase by \( 360^\circ / n \), available from the scheme. The oscillation frequency \( \omega_0 \) is given by

\[
\omega_0 = \frac{1}{T} \tan \left( \frac{\pi}{2n} \right) \tag{6}
\]

Eq.(7) provides the oscillate condition while the oscillation frequency \( (\omega_0) \) is given the value of \( n \ (1, 2, 3, \ldots) \) by

\[
k = 1 \tag{7}
\]

Return to the basic odd-phase system of Fig.1, consider the case \( n \equiv 3 \). This represents a three-phase MSO, in Eq.(6) the oscillation frequency yields

\[
\omega_0 = \frac{1}{\sqrt{3}T} \tag{8}
\]

B) CMOS Current-controlled Current Conveyor (CCCI)

A CCCI is a versatile active building block which including 3-ports, X, Y and Z. The matrix-relationship between voltage and current variables among port X, Y and Z of ideal CCCI can be described by the following matrix equation.

\[
\begin{bmatrix}
0 & 1 & 0 \\
1 & 0 & 0 \\
0 & 0 & 1
\end{bmatrix}
\begin{bmatrix}
v_x \\
v_y \\
v_z
\end{bmatrix}
= \begin{bmatrix}
v_i \\
v_i \\
v_i
\end{bmatrix} \tag{9}
\]

Where the positive and negative signs of the current \( i_x \) denoted the positive (CCI+), and negative (CCI-), respectively, and \( R_i \) is an intrinsic resistance of CCCI. The circuit configuration for conventional CMOS CCCI is illustrated in Fig.2(a) based on complementary source follower [19] and its equivalent circuit is shown in Fig.2(b). The X-terminal impedance is calculated by

\[
R_i \approx \frac{1}{g_{m9} + g_{m10}} \tag{10}
\]

Where \( g_{m9} \) denotes a transconductance of transistor number \( i \). If matched transistors \( M_9 \) and \( M_{10} \) are supposed, \( g_{m9} = g_{m10} \), then

\[
R_i \approx \frac{1}{8\mu C_{ox} (W/L) I_t} \tag{11}
\]
Whereas $\mu$, $Cox$, $W$ and $L$ are respectively surface mobility, oxide capacitance, channel width and length of MOS transistor, $M_6$ and $M_{10}$. Consequently, $g_m$ can be tuned electronically by current bias $I_g$.

C) CCCII-based current-mode all-pass network

A CCCII-based APN uses a grounded capacitor with electronic tunability without any resistors which suitable for modern compact integrated circuit. The APN or first order all-pass filter is a main building block that is realized by MO-CCCII. A CCCII-based current-mode APN provides current output and input as shown in Fig.3.

Assuming $R_{c2}=R_{c3}=R_c$, completed current-mode transfer function of CCCII-based APN can be expressed as

$$T_{av}(s) = \frac{s}{i_m} = -k \frac{1-sT}{1+sT}; \quad R = R_{c1}/R_c; \quad T = CR_c$$

where $k$ is the current gain, $R$ is the resistance, $T$ is the time constant, $C$ is the capacitance, and $\omega$ is the angular frequency. The three CCCIIIs have been used for achieving each all-pass section as shown in Fig.3. It can be seen that stage-gain ($k$) of each all-pass section is electronically adjustable by $R_c$. Note that, APN is easily directed cascadable to the next current-mode succeeding stage.

III. MULTIPHASE SINUSOIDAL OSCILLATOR

A three-phase sinusoidal oscillator based on Fig.1 was implemented for confirmed the theory as shown in Fig.4. In order to simply adjustment method, CCCII2, CCCII3 are biased identically by $I_{B2}=I_{B3}$ but CCCII1 is biased independently by $I_{B1}$ for achieving the certain condition of $k=1=R_{c1}/R_c=I_{T1}/I_{B1}$. Each inverting stage (APN1-APN3) provides high output impedance that drives to the succeeding stage so these results in three cascaded of first-order APN inverting stages given by

$$T(s) = \frac{i_1}{i_m} = \frac{1-sRC}{1+sRC}$$

and frequency of oscillation will become

$$\omega_0 = \frac{1}{3\sqrt{2}C}$$

Following the proposed configuration in Fig.4, both of voltage and current output can be provided without changing circuit topology. By the addition of $n$ unity current gain inverters at every CCCII’s, the system can generate $2n$ even phases. Using the same configuration, voltage output is simultaneously obtained at port X of every CCCII’s.

IV. NON-IDEAL ANALYSIS

Matrix equation in the standard notations, the CCCII as shown in Fig.5 can be non-ideal characterized by [20]

$$\begin{bmatrix} i_v \beta \beta \delta \delta \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & v_y \\ v_y & \beta & R_c & 0 \\ i_x & 0 & \pm \alpha & 0 \\ v_z & 0 & 0 & v_z \end{bmatrix} \begin{bmatrix} i_v \\ i_y \\ i_x \\ v_z \end{bmatrix}$$

where $\alpha = 1 - e$; $|e| << 1$, $e$ represents the current tracking error and $\beta = 1 - \delta$; $|\delta| << 1$, $\delta$ represents the voltage tracking error. The intrinsic resistance $R_i$ is proportional to its bias current $I_{Bi}$ without effect from tracking errors. The CCCII-based current-mode APN as shown in Fig.3 by assuming the matched condition of $R_{c1}$ and $R_{c2}$ ($R_{c2}=R_{c3}=R_c$) can be rewritten the non-ideal transfer functions as

$$T_{av} = \frac{i_c}{i_m} = -\alpha \beta k$$

Considering Fig.3 based on Eq.(16), assumed $n$-stages with non-ideal phase shift $(\phi)$, the total of phase $2\pi$ for 1 cycle can be expressed as

$$\phi = 2\pi n = 2\pi \left( -\tan \left( \frac{1}{\alpha} \right) \right) = -2\pi$$

The non-ideal oscillation frequency $\omega_0$ is given by

$$\omega_0 = \frac{1}{nRC} \tan \left( \frac{\pi}{\alpha} \right)$$

Reanalysis the oscillate condition using the similar analysis as section II, the oscillate condition is found to be

$$k = \frac{1}{n\alpha \beta}$$

From Eq.(18), it can be seen that the oscillation frequency is received small effects from the CCCII current tracking error ($\epsilon$). From Eq.(19), the oscillate condition ($k$) of proposed oscillator has been affected by voltage and current tracking errors ($e$ and $\delta$) depend on decreasing of both voltage gain and current gain in order to higher frequency operation. Another error would be found that if the parameter $R_{c1}$ and $R_{c3}$ mismatched.

Considering in term of parasitic elements effect, reanalysis only 1 stage of CCCII-based APN as shown in Fig.3 using the CCCII non-ideal equivalent circuit in Fig.5 [20] while the $\beta_s$ and $\omega_0$ values are very close to unity for taking into parasitic elements consideration which depicted in Fig.5, the non-ideal analysis of current transfer function is found to be
\[ i_d = \frac{R_x \alpha \beta \left( R_x R_y - R_x R_z \right) - s \left( R_x R_y R_z + R_x R_y R_c \right)}{R_x} \]  

(20)

Whereas \( D(s) = \left( R_x R_y + 2R_x R_y + 2R_x \right) + \left( R_x R_y R_z + R_x R_y R_c + 2R_x R_y R_z + 2R_x R_y R_c \right) + s^2 R_x R_y R_z \left( C + C_c \right) \)

The biased current of every CCCIIs are roughly identical supposed for achieving stage-gain \( k=1 \). Port X resistance of every CCCIIs are therefore approximately equaled. Considered at port X, port Y and port Z, the resistance of port Y and port Z are definitely larger than port X resistance. Likewise, the capacitance at port Y and port Z are definitely smaller than \( C \) value. Eq.(22) can be therefore simplified to

\[ i_{dN} \approx \frac{1 - s R_x C}{1 + s R_x C + s^2 R_x R_c C} \]  

(21)

Eq.(21) illustrates that the effects of parasitic elements are depended on two poles. First high-frequency poles which located in very far from the origin and second low-frequency poles (dominant poles) can respectively be expressed by

\[ \omega_1 = \frac{1}{R_x \sqrt{2 C_c C}} \]  

(22)

and the dominant pole is

\[ \omega_2 = \frac{1}{C R_x} \]  

(23)

V. SIMULATION RESULTS

The proposed circuits simulates by using PSpice circuit simulation program. The NMOS and PMOS transistors were simulated for CCCI based on the parameters of the TSMC MOSIS 0.25\( \mu \)m in Table.1 and aspect ratios in Table.2 under \( \pm 2 \)votls power supplies. The electronic tunability phase response of proposed unity gain CCCI-based first-order APN by assuming the same current biased \( (I_b) \) of all CCCIIs is exhibited in Fig 6. Adjusting of APN stage-gain characteristic is illustrated in Fig.7 for gain=1, 2 and 4, respectively. The same phase response characteristic of different gains can be observed.

Table 2. Transistors aspect ratio of CMOS CCCI

<table>
<thead>
<tr>
<th>Transistors</th>
<th>W(( \mu )m)</th>
<th>L(( \mu )m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M3, M7, M11, M13, M15, M17, M21</td>
<td>5</td>
<td>0.5</td>
</tr>
<tr>
<td>M2, M4, M8, M12, M14, M16</td>
<td>15</td>
<td>0.5</td>
</tr>
<tr>
<td>M5, M9</td>
<td>2</td>
<td>0.5</td>
</tr>
<tr>
<td>M6, M10</td>
<td>4</td>
<td>0.5</td>
</tr>
</tbody>
</table>

Fig.6 Phase response of CCCI-based APN with varying of \( I_b \)

Fig.7 Maximum magnitude and phase response of CCCI-based all-pass

For odd structure \( n = 3 \), the start of the oscillation is caused by a fast decaying sinusoidal function. To demonstrate that the oscillations are assumed by power-on situation with very short-times current (50\( \mu \)A/1ps) attacked into a node of CCCI. For \( n=3 \), the oscillation output results are obtained by the following condition, \( C=10pF \), \( I_b1=91.5\mu A \) and \( I_b2=I_b3=100\mu A \). The 4.5MHz sinusoidal signal of 6-phase current outputs is illustrated in Fig.8. It found that 60° equally phase difference of each output with a small offset according to CCCI characteristic. The three-phase voltage output is illustrated in Fig.9 with 120° equally phase difference of each output.

Proposed sinusoidal output signal of Fig.9 by using \( I_b=100\mu A \) which is also contributed to prove of the low THD characteristic. The very small of 2\( ^{nd} \) and 3\( ^{rd} \) harmonic frequency components are about 981.553\( \mu V \)
and 361.572μV, respectively, while fundamental frequency at 4.5MHz about 121.215mV or low THD around 0.86% according to the theory of high-order network as shown in Fig.10 that can be observed. The frequency output while changing capacitor and varied CCCII’s current biased are plotted in Fig.11.

![Fig.10 Simulated results of 4.5MHz spectrum](image1)

![Fig.11 Oscillation frequency while CCCII biased and capacitor changing](image2)

V CONCLUSION

A new simple structure of current-controlled MSO based on CMOS CCCII APN structure has been presented. Proposed APN is able to adjust its stage-gain electronically. This system consists of n-cascaded all-pass first-order stages and produces an even-number or an odd-number of equal-amplitude from high impedance sources equally spaced in-phase output currents. Low THD less than 0.9% can be obtained by using the high-order network function. Both voltage and current outputs can be obtained simultaneously.

REFERENCES


