CMOS-based High-frequency Tunable Current-mode Continuous-time Universal Filter

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Abstract—This paper proposes a new realization of multiple inputs single output current-mode universal filter based on CMOS transistor level. Two-type of lossy and lossless integrators are used to realize for the two integrators loop filter structure. Only eight NMOS and a CMOS-based grounded capacitor are constructed as a current-mode universal filter. The frequency response can be controlled based on bias currents. Four decades of frequency controllable with five types of standard filter such as low-pass, high-pass, band-pass, band-reject and all-pass response can be obtained. Due to use of transistor level, high frequency can be operated up to 100MHz. The low-power supply, 1V is used for the proposed filter with low-power consumption around 9.12μW at 1μA bias current. The simulations results are totally agreed with theoretical by using SPICE.

Keyword: High-frequency, Universal Filter, CMOS, Tunable

I. INTRODUCTION

High performance active filters have been received much attention. In filter circuit design, current-mode filters are popular. These current-mode filters have many advantages compared with their voltage-mode counterparts. Due to many advantages of current mode filters, they are used in many filter circuit design. The benefits of current-mode circuits are confirmed, for example, high-frequency response, compactness fabrication, low-power and simply sum/subtract.

The filter circuit has been discovered for a long time based on a biquadratic function [1]. A biquadratic filter is a basic second-order function block for realizing high-order filter functions. In high-frequency continuous-time integrated filter design, one of the most successful methods is the OTA-C approach. The current-mode realizations have been rapidly introduced in many years. The design of current-mode filters employ active devices such as, current followers (CFs) [2], second generation current conveyors (CCIs) [3-5] and operational transconductance amplifiers (OTAs) [6-11] have been introduced in the previous works. Analytic synthesis of filter functions based on OTA-C [12], [13] and DVCC [14] are introduced.

Several previous filters have been proposed based on active devices with electronic tunable in several megahertz frequency response. Frequency response is actually limited by bandwidth of active device. High power supplies are needed with high power consumption. Narrow tunable of frequency range as small as two decade range. At least one of these needs connection of resistors [3], [5] or floating capacitors or resistors [2]. They are therefore not suitable in IC productions.

Continuous-time filters operating at cutoff frequencies exceeding 10 MHz constitute a large potential market in applications such as video signal processing and magnetic disk-drive read-channel systems [15]-[20]. This paper proposes a multiple inputs single output (MISO) current-mode universal filter based on CMOS technology. Only eight NMOS transistors and 2 CMOS-based grounded capacitors are realized for the proposed filter. The synthesis algorithm of two integrators (lossy and lossless integrators) loop is used as a filter prototype. Two NMOS transistors are realized for a lossy integrator and 6 NMOS transistors are realized for a lossless integrator.

The proposed filter is enabled to provide the following benefits; high-frequency operation, electronic tuning, low components count, low voltage, low power consumption and able to further fabricate in IC production. The low sensitivities within ±0.5 of the passive and active elements are obtained. The filter characteristic functions including low-pass (LP), high-pass (HP), band-pass (BP), band-reject (BR) and all-pass (AP) can be obtained without changing the circuit topology. The operating principles of the continuous-time current-mode lossless and lossy integrators are presented in Section 2 including a first-order analysis of its performance characteristics. Design considerations for implementing current-mode continuous-time universal filter are described in Section 3. The discussion of high-order effects that impact its speed and accuracy are discussed in Section 4. The simulation results by using SPICE, layout and post-layout simulation based on 0.25μm are performed and summarized in Section 5 and conclusions are given in Section V.

II. CIRCUIT DESCRIPTION

A) CMOS-based integrators

Integrator is a useful building block which needs to realize high-order filter functions. Lossless integrator can
be designed by several techniques. This lossless integrator technique uses only 6 MOS transistors based on a negative feedback of lossy integrator block as shown in Fig.1 [22-23]. In order to facilitate our discussion, a small-signal model of the integrator in Fig. 1 is recalled in the below equivalent circuit in which the output conductances are neglected. Their input–output relationship is given by the expression. Applying KCL at nodes 1, 2, and 3 yields

\[ I_{in} = g_{m1} V_i + g_{m2} V_i \]  
\[ g_{m1} V_i = - (g_{m4} + s C_1) V_i \]  
\[ I_{out} = - g_{m3} V_i \]  

Fig.1 CMOS current-mode lossless integrator circuit

Substitute Eqs.(1) and (2) into (3), the current transfer function gives

\[ I_{out} = \frac{g_{m3} g_{m8}}{g_{m4} g_{m6} - g_{m3} g_{m7} + s g_{m7} C_2} \]  

\[ D(s) = g_{m8} g_{m6} - g_{m3} g_{m7} + s g_{m7} C_2 \]  

Fig.3 Two integrators loop function block diagram

B) Realization of universal filter

The block diagram in Fig.3 shows the BP function that can be implemented by lossless and lossy integrators in Fig.4. The transfer function can be written as

\[ Y(s) = \frac{s A}{s^2 + s A + AB} \]  

Fig.4 Proposed CMOS current-mode universal filter

The lossless integrators can be realized by many kinds of active devices. Due to current-mode benefits, proposed filter is designed in current-mode approach. The limitation of bandwidth is a highlight problem for high-frequency application. The proposed current-mode universal filter is realized by using lossless and lossy integrators in Fig.1 and 2 based on MOS transistors with grounded capacitors. By the design, it accommodates the attractive benefits such as low-voltage, wide-range electronic tunability, low-component count and high-frequency operation. By straightforward analysis, the current output function can be expressed as Eq. (6).

\[ I_{out} = \frac{g_{m8} g_{m6} - g_{m3} g_{m7} - s (g_{m8} g_{m7} C_2)}{I_{in}} + g_{m8} g_{m6} s C_2 \]  

\[ D(s) = g_{m8} g_{m6} - g_{m3} g_{m7} + s (g_{m8} g_{m7} C_2 - C_1 g_{m8} g_{m7} + C_1 g_{m7} g_{m6} + s g_{m7} C_2) + s^2 (g_{m8} g_{m7} C_2) \]  

Supposed that, the transistors are matched with the following conditions, \( g_{m1} = g_{m2} = g_{m3} = g_{m4} \) and \( g_{m8} = g_{m6} = g_{m7} = g_{m6} = g_{m7} = g_{m8} \), then the output current functions is satisfied by

\[ I_{out} = \frac{-s \left( g_{m8} g_{m7} C_2 \right) + \left( g_{m8} g_{m7} C_2 \right) + D(s) I_1}{D(s)} \]  

Where \( D(s) = s^2 + \frac{g_{m8} g_{m7} C_2}{C_1} + g_{m8} g_{m8} s C_2 \). It can be seen that the proposed filter can realize to five types of standard biquadratic filter which summarized conditions are:

1. The LP response can be realized when \( I_1 = I_3 = 0 \) and \( I_2 = I_{in} \).
2. The BP response can be realized when \( I_2 = I_3 = 0 \) and \( I_1 = I_{in} \).
3. The HP response can be realized when \( I_1 = I_2 = I_3 = I_{in} \).
4. The BR response can be realized when \( I_2 = 0 \) and \( I_1 = I_{in} \).
5. The AP response can be realized when \( I_2 = 0 \) and \( I_1 / 2 = I_3 = I_{in} \).

Considering the denominator \( D(s) \) and the characteristic equation \( D(s) = s^2 + \frac{s^2 A}{Q^2} + \omega^2 \), the
Concerning parameters including $\omega_p$ and $Q_p$ are given below

$$\omega_p = \frac{\frac{g_m S_{ab}}{C_{C}}}{C_{C}}$$

(10)

and

$$Q_p = \frac{\frac{g_m S_{ab}}{C_{C}}}{C_{C}}$$

(11)

From Eq. (10) and (11), the following $\omega_p$ and $Q_p$ parameters can be rewritten in term of current biases as

$$\omega_p = \frac{2 \mu C_{in} W}{L} \left[ \frac{I_{D}}{I_{D}} \right]_{g} \left[ \frac{I_{D}}{I_{D}} \right]_{C}$$

(12)

and

$$Q_p = \frac{I_{D} C_{g}}{I_{D} C_{C}}$$

(13)

III. SENSITIVITY

Another filter performance can be indicated by its sensitivities. The sensitivities with respect to active and passive elements are according to the frequency response $S_{op}$ and quality factor $Q_{op}$, where $x$ is active and passive elements. The low active and passive sensitivities of $\omega_p$ and $Q$ are shown as

$$S_{op}^x = -S_{op}^x = -0.5$$

(14)

$$S_{op}^0 = -S_{op}^0 = -0.5$$

(15)

IV. EFFECTS OF THE PARASITIC ELEMENTS

Equations (9) to (13) have been obtained by considering the ideal description of the transistors. Drain-source of parallel conductance and capacitance effects. The low active and passive sensitivities of $\alpha$ and $\rho$ parameters can be rewritten in term of current biases as

$$\omega_p = \frac{\frac{g_m S_{ab}}{C_{C}}}{C_{C}}$$

(10)

and

$$Q_p = \frac{\frac{g_m S_{ab}}{C_{C}}}{C_{C}}$$

(11)

From Eq. (10) and (11), the following $\omega_p$ and $Q_p$ parameters can be rewritten in term of parasitic conductance and capacitance effects.

$$D_{l_q} (s) = s^2 C_{g} \left( g_{ds} + g_{ds} + 2 g_{ds} \right) + s \left[ C_{1} \left( g_{ds} g_{ds} + 4 g_{ds} g_{ds} \right) + C_{1} \left( g_{ds} g_{ds} + g_{ds} \left( g_{ds} + g_{ds} \right) + g_{ds} \left( g_{ds} + 2 g_{ds} \right) \right] + g_{ds} g_{ds} \left( g_{ds} + 4 g_{ds} \right) \right)$$

(18)

From Eq. (18), the parameters of the non-ideal proposed filter in term of parasitic conductance $g_{ds}$ are expressed as

$$\omega_p = \frac{\frac{g_m S_{ab}}{C_{C}}}{C_{C}}$$

(19)

$$Q_p = \frac{\frac{g_m S_{ab}}{C_{C}}}{C_{C}}$$

(20)

Due to the parasitic effects, undesirable factors are yielding in the transfer functions of the filter. Equations (19)-(20) show that such factors can be neglected by satisfying the following conditions.

$$5 g_{ds} << g_{ds}$$

(21)

The second consideration, taking the parasitic capacitance $C_{p}$ of the MOS transistors from Fig.6 into account, and supposed that $C_{p} = C_{p} = C_{p} = C_{p} = C_{p}$ and $C_{p} = C_{p} = C_{p} = C_{p} = C_{p} = C_{p} = C_{p}$, the current transfer function of proposed filter can be rewritten as

$$I_{D} = s^2 g_{ds} g_{ds} + s^2 C_{g} \left( g_{ds} g_{ds} + 2 g_{ds} \right)$$

(22)

$$\frac{D_{l_q}}{s} = \frac{g_m S_{ab}}{C_{C}}$$

(23)

$$D_{l_q} (s) = s^2 g_{ds} g_{ds} + s^2 C_{g} \left( g_{ds} g_{ds} + 2 g_{ds} \right)$$

(24)

From Eq. (24), the parameters of the non-ideal proposed filter in term of parasitic capacitance $C_{p}$ are expressed as

$$\omega_p = \sqrt{\frac{g_m S_{ab}}{C_{C}} + 2 g_{ds} g_{ds} + 2 g_{ds} g_{ds} + 2 g_{ds} g_{ds}}$$

(25)

$$Q_p = \sqrt{\frac{g_m S_{ab}}{C_{C}} + 2 g_{ds} g_{ds} + 2 g_{ds} g_{ds} + 2 g_{ds} g_{ds}}$$

(26)

Due to the parasitic effects, undesirable factors are yielding in the transfer functions of the filter. Equations (25)-26) show that such factors can be neglected by satisfying the following conditions.

$$10 C_{p} << C_{1}, C_{2}$$

(27)

V. SIMULATION RESULTS

The proposed current-mode high-frequency universal filter can be confirmed the characteristics and its performance by SPICE based on CMOS technology. The NMOS is constructed with +1V power supplies. The model parameters of the TSMC MOSIS 0.25μm process as listed in Table2 with W/L=1μm/0.25μm for M1-M8.
Table 2 Model Parameter of MOS transistors used for PSpice simulation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>W1=300, L=0.1um, P=0.7</td>
</tr>
<tr>
<td>M2</td>
<td>W2=300, L=0.1um, P=0.7</td>
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<tr>
<td>VTO</td>
<td>0.5V</td>
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<td>( \gamma )</td>
<td>0.15</td>
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<tr>
<td>( \theta )</td>
<td>0.95</td>
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<td>( \eta )</td>
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<tr>
<td>( \theta' )</td>
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<tr>
<td>( \eta' )</td>
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<td>( \beta )</td>
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<tr>
<td>( \alpha )</td>
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<td>( \delta )</td>
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<td>( \epsilon )</td>
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<td>( \theta'' )</td>
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<td>( \epsilon''' )</td>
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</table>

Gain (dB)

Fig.7 LP, HP, BP and BR magnitude responses

Gain (dB)

Fig.8 AP magnitude and phase responses

Gain (dB)

Fig.9 Electronic tunable characteristics of filter using BP

The electronically controlled frequency response of proposed filter can be achieved by giving the identical conditions of \( g_{m1} = g_{m2} \) by using \( I_{p1} = I_{p2} = I_p \) and capacitors \( C_1 = C_2 = C \). The characteristic results of proposed filter are shown in Fig.7. Various filter characteristics of proposed circuit are supposed the following conditions which are \( I_p = 100 \text{mA} \) and identical capacitors around 0.03pF. The characteristic of 4 types of standard filters (LP, HP, BP and BR) can be obtained around 10MHz. Figure.8 shows magnitude and phase responses of AP filter at 10MHz frequency response. Figure.9 exhibits the wide range electronic tunable characteristics of frequency response (\( f_p \)) by using BP and BR filters, respectively. Biased current (\( I_p \)) is varied from 1nA to 1\( \mu \text{A} \), then \( f_p \) is varied from 100 kHz to 100MHz.

VI. CONCLUSION

This paper presents a design of high-frequency multiple-inputs single-output universal filter by using only 8 MOS transistors. Five types of standard filter function can be obtained. Low power supply and low power consumption at 100\( \mu \text{A} \) current biased are respectively obtained around 1V and 9.12\( \mu \text{W} \). High-frequency around up to 100MHz with 4 decades of wide range tuned. This proposed filter is offered to use in the telecommunications, video applications and general high-frequency purposes.

REFERENCES


