A single power supply CMOS four-quadrant analog multiplier

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Abstract
This paper proposes a single power supply analog multiplier design based on the quarter-square algebra in CMOS technology. The number of transistors is decreased, the performances are better than the previous papers [1]-[7].

Introduction
The analog multipliers are useful in analog signal processing. They can be adapted for using in analog filter, frequency doubler, modulator and etc. The developments of analog multiplier have been made from bipolar transistors [8] and then using with MOS transistors [1]-[7]. This paper proposes a design technique to use MOS transistors based on the quarter-square algebra of ref. [1]. Consider the differential summing circuit, the transistors operate in saturation region with narrow dynamic range. It uses the differential pairs, then the transistors operate with narrow dynamic range as in ref. [2]. The V-I converter operates in non-saturation region, therefore the circuit operate with error in the case of V is less than threshold voltage. Two sets of power supply, level shifter circuit are required for improving this circuit for operating in saturation region with wide dynamic range. This paper proposes a design technique with 5 volts power supply to obtain the better performances and overcomes the disadvantages. The simulation with experimental results are also presented. The level 2 worst case model of European Silicon Structure (ES2) is used for the simulation.

Theory
The four-quadrants analog multiplier is widely used and based on the quarter-square algebraic identity as shown in Fig. 1.

![Fig. 1. The quarter-square algebraic identity multiplier technique.](image-url)
The structure as shown in Fig.1 consists of additional, subtractional and squaring circuits.

- Additional and subtractional circuits

The summing signal circuit uses the principle the transistors operation in saturation region as shown in Fig.2. The drain current of MOS transistor is written as:

\[ I_d = k \left( V_{gs} - V_T \right)^2 \text{ for } \left( V_{gs} - V_T \right) \leq V_{ds} \]  

(1)

when \( k = \frac{\mu C_{ox}}{2} \left( \frac{W}{L} \right) \)

![Image of NMOS inverter circuit](image)

Fig.2. The NMOS inverter circuit.

The circuit as shown in Fig.2, it found that:

\[ I_{d1} = \frac{\mu C_{ox}}{2} \left( \frac{W}{L} \right)_1 \left( V_A - V_{os} - V_{TN} \right)^2 \]  

(2)

\[ I_{d2} = \frac{\mu C_{ox}}{2} \left( \frac{W}{L} \right)_2 \left( V_B - V_{TN} \right)^2 \]  

(3)

when \( I_{D1} \) and \( I_{D2} \) are the drain current of M1 and M2, respectively. This circuit acts as an inverter. Suppose that \( I_{D1} = I_{D2} \) thus the output voltage \( V_{OS} \) will be in the function of subtraction as in equation (4).

\[ V_{os} = V_A - V_{MN} + \left( V_{MN} - V_T \right) \sqrt{\left( \frac{W}{L} \right)_2 \left( \frac{W}{L} \right)_1} \]  

(4)

The condition of Fig.1 is satisfied because of M1 and M2 must operate in saturation region. This condition can be done by using various techniques as in Ref.[1]. The transistors in the proposed technique is less than in the previous paper and uses only +5 volts power supply. This paper proposes to use voltage level shifter circuit to implement this proposed multiplier circuit and uses only single power supply.
Voltage level shifter circuit

The transistors M1 and M2 of NMOS inverter as shown in Fig. 2 must be operated in saturation region, it will satisfy the equation (4). Therefore, the circuit must have the negative power supply, the threshold voltage and it can be written as:

$$V_A \leq (V_{DD} + V_{TN})$$

(5)

The values in the equation (5) is limited by $(V_{DD} + V_{TN})$ for the transistor M1, but the transistor M2 will have the problem according to $V_{DD} > 2V_{TN}$. Thus, the equation should be:

$$\left( V_B - V_{TN} \right) \leq V_{OS}$$

(6)

The accepted condition should be $\left( V_B - V_{TN} \right) = V_{OS}$ or $V_B > V_{TN}$. Suppose that $V_{OS} = V_{TN}$, therefore $V_B = 2V_{TN}$. The input voltage ($V_I$) of the squaring circuit must be greater than $V_{TN}$. The equations can written as follows:

$$\left( V_B - V_{TN} \right) > V_{TN}$$

(7)

$$V_B > 2V_{TN}$$

(8)

The voltage level shifter uses the principle of saturated region of MOS transistors with a constant current circuit as shown in Fig. 3.

![Fig. 3. The voltage level shifter circuit.](image)

The drain current of transistor in Fig. 3 is equal to $I_B$ and can be written as:

$$I_D = -I_B = -k_p \left( V_B - V_{TN} \right)^2$$

(9)

or

$$V_B' = V_B + \sqrt{\frac{I_B}{k_p}}$$

(10)

The new voltage level ($V_B'$) depends on $I_B$ and $V_{TP}$. It is unnecessary to use dual-power supply. Thus, the +5 volts power supply is needed. The circuits in Figs. 2 and 3 are symmetrical combined together, therefore the circuit in Fig. 4 is obtained.

![Fig. 4. The differential summing circuit after combining Figs. 2 and 3.](image)
From Fig.4, the output voltage equation can be written as:

$$
V_{OS1} = V_{TR} + \frac{V_{A}}{2} + \frac{I_{I2}}{k_p} - V_{TN} + \left[ V_{TN} - \left( \frac{V_{TR}}{2} + \frac{I_{I2}}{k_p} \right) \right] \frac{W/L}{2}, \quad (11)
$$

$$
V_{OS2} = V_{TR} + \frac{V_{A}}{2} + \frac{I_{I2}}{k_p} - V_{TN} + \left[ V_{TN} - \left( \frac{V_{TR}}{2} - \frac{I_{I2}}{k_p} \right) \right] \frac{W/L}{2}, \quad (12)
$$

Finally, the differential output voltage can be obtained as:

$$
V_{OS} = V_{OS1} - V_{OS2} = V_{A} - V_{T} \sqrt{\frac{W/L}{2}}, \quad (13)
$$

- The differential squaring circuit

The differential squaring circuit in this paper will use the principle of Square's law of MOS transistors which operate in saturation region. The drain current is in the form of square value as shown in equation (2), its structure is shown in Fig.5. The circuit in Fig.5 is only half circuit, therefore the drain currents of M1 and M2 can be written as:

$$
I_{D1} = k_n (V_1 - V_{TN}) \quad (14)
$$

$$
I_{D2} = k_n (-V_1 - V_{TN}) \quad (15)
$$

![Fig.5. The squaring circuit.](image-url)

The voltages $V_1$ and $-V_1$ are differential input, thus the output squaring voltage ($V_{OSQ}$) is obtained as:

$$
V_{OSQ} = V_{DD} - k_n R_1 \left[ 2V_{TN}^2 + 2V_1^2 \right] \quad (16)
$$

The DC component can be omitted by connecting the differential output as shown in Fig.6.

![Fig.6. The differential squaring circuit.](image-url)

From Fig.6, both of the outputs are:

$$
V_{OSQ} = V_{DD} - \frac{R_1 \mu C_{OS}}{2} \left( \frac{W}{L} \right) \left[ 2V_{TN}^2 + \frac{V_1^2}{2} \right] \quad (17)
$$
\[ V_{osq2} = V_{dd} - \frac{R_i \mu C_{ox}}{2} \left( \frac{W}{L} \right) \left( 2V_{th}^2 + \frac{V_{dd}^2}{2} \right) \]  

(18)

Thus, the differential output is:

\[ V_{osq} = V_{osq1} - V_{osq2} = \frac{R_i \mu C_{ox}}{4} \left( \frac{W}{L} \right) \left( V_A^2 - V_B^2 \right) \]  

(19)

**Simulating results**

The completed circuit of the proposed single power supply CMOS four-quadrant analog multiplier is shown in Fig. 7, and the output voltage of this circuit is

\[ V_o = \mu C_{ox} R_i \left( \frac{W}{L} \right) \left( \frac{W}{L} \right) V_A V_B \]  

(20)

Fig. 7. The proposed circuit.

Fig. 8. The measurements of the characteristic curves of the proposed analog multiplier circuit (a) \( V_B \) is a parameter and (b) \( V_A \) is a parameter.
This circuit consists of 12 NMOS and 4 PMOS transistors with \((W/L) = 20/10\) except M5, M6, M12 and M13 use \((W/L) = 100/10\). \(I_{D1}\) and \(I_{D2}\) are set equal to 150 \(\mu\)A and 20 \(\mu\)A, respectively. The electrical simulations use the level 2, worst case model of European Silicon Structure for \(V_{TN} = 1.07\) volts, \(V_{TP} = -0.8\) volts, \(\mu_p C_{ox} = 54.38\) \(\mu\)A/\(V^2\), \(\mu_n C_{ox} = 21.26\) \(\mu\)A/\(V^2\) and \(R_f = 500\) Ohms. The PSpice program is used for all of simulations. The characteristic curves of proposed single power supply CMOS four-quadrant analog multipliers are shown in Fig. 8.

![Frequency Response](image)

**Fig. 9.** Frequency response of proposed multiplier.

Fig. 9 shows the frequency response of the proposed multiplier circuit, the bandwidth is quite wide about 50 MHz.

**Conclusions**

An CMOS four-quadrant analog multiplier operating with single power supply is presented. Its structure is easy to implement, the linearity error of output voltage is about 0.6%. It uses 16 transistors and 4 constant current circuits and the frequency response is quite high.

**References**