Single Low-Supply and Low-Distortion CMOS Analog Multiplier

Pipat Prommee1 Montri Somdunyakanok2 Krit Angkaew3 Arkhom Jodtang1 and Kobchai Dejhan1
1Faculty of Engineering and Research Center for Communication and Information Technology
King Mongkut’s Institute of Technology Ladkrabang, Bangkok 10520, Thailand
Tel: 66-2326-4238, 66-2326-4242, Fax:66-2326-4554,
2Electrical Engineering Department, Faculty of Engineering,
Siam University, Bangkok 10520, Thailand.
3Industrial Electrical Technology Department, Faculty of Engineering
King Mongkut’s Institute of Technology North Bangkok, Bangkok 10800, Thailand
Email: {pipat, kobchai}@telecom.kmitl.ac.th, monsom@siamu.com

Abstract— A single low-supply CMOS Analog Multiplier based upon ohmic region of MOS transistors is presented. This paper describes a method to force the drain-source voltage \( V_{DS} \) of MOS transistors to operate in ohmic region. The achieved circuit can be used a single low-power supply. The complete circuit contains 20 transistors and 8 current sources using a low-power supply +1.5 volts. This circuit has high performance with very high-linearity and low-distortion. The achieved input dynamic range operation is ±400mV, the linearity error is smaller than 0.1% and total harmonic distortion is smaller than 0.25% for input range 800mVp-p.

Keyword— CMOS Analog Circuit, Analog Multiplier, Low-Supply

I. INTRODUCTION

The analog multiplier cells have been rapidly proposed in recent years [5-9]. The several methods are used for implemented. This paper presents a new approach for implement an analog multiplier. This proposed technique is based on ohmic region of MOS transconductance circuit that under forcing of drain-source voltage. The particular sub-circuits are used in this approach for achieving the complete circuit such as: voltage-level shifter, shunt-feedback buffer and ohmic transconductance element. A single low-power supply can be use for +1.5V with linear range operation within ±400mV.

II. PRINCIPLES

A Voltage-Level Shifter Circuit

This circuit employs a PMOS and a current source as shown in Fig.1. The transistor is operated in saturation region can be described the drain current as shown in Eq. (1). The output voltage can be written as Eq. (2)

\[
I_B = k_p \left(V_B - V_i - |V_{TP}|\right)^2
\]

Where 
\[
k_p = \frac{\mu_p C_{OX}}{2} \left(\frac{W}{L}\right)
\]

\[
V_B = V_i + |V_{TP}| + \sqrt{\frac{I_B}{k_p}}
\]

Fig 1 Voltage-Level Shifter Circuit

B. Shunt-Feedback Buffer Circuit

Fig. 2 shows shunt-feedback buffer circuit [1]. It contains the 2 current sources and 3 transistors. The transistor \( M_1 \) is using for supply its source voltage, \( M_2 \) using for supply current at node \( V_i \) and \( M_3 \) is done for output current. All transistors are operated in saturation region. So, the voltage output can be written as follows :
The output current $I_O$ equals $I_2 - I_1$ obtained from current mirror $M_3$. However, the bias $I_1$ can be cancelled by symmetry differential scheme because $I_1$ is constant, while the transistors of both sides must be identical. Consider circuit Fig. 2, current source $I_1$ is the drain current of $M_1$ and $I_2$ is the total current source of circuit. While input voltage ($V_C$) is applied in gate of $M_1$, source voltage is appearred. The enough current should be supplied in case of load connected at node $V_O$. Thus, $M_2$ and $I_2$ are employed to supply current. This proposed circuit does not use $I_2$ because it can replace by ohmic transistor that cause main transconductance elements, so the $V_O$ must be set to lowest since $V_O$ complied to $V_{DS}$ in order to operated transistor in ohmic region that must be within a condition of $G_{SSV}$.

**III. LOW-SUPPLY OHMIC TRANSCONDUCTANCE**

The principle of MOS pairs transistor in Fig.3 are identical operation in ohmic region and perfect matched that can be written as follows:

$$I_{D1} = \mu_N C_{ox} \left( \frac{W}{L} \right) \left( V_{GS1} - V_{TN} - \frac{V_{DS1}}{2} \right) V_{DS1} \quad (4)$$

$$I_{D2} = \mu_N C_{ox} \left( \frac{W}{L} \right) \left( V_{GS2} - V_{TN} - \frac{V_{DS2}}{2} \right) V_{DS2} \quad (5)$$

$$V_O = V_C - \frac{I_1}{\sqrt{k_n}} - V_{TN} \quad (3)$$

The drain voltage $V_{DS}$ of $M_2A$ and $M_2B$ are equalled, which are controlled by $V_C$. The $M_{1A}$ and $M_{1B}$ used for shift-up the input voltage for gate voltage of $M_2$ according to the ohmic condition. The output current is mirrored from $M_{4A}$, $M_{4B}$ by $M_{5A}$, $M_{5B}$. The current $I_1$ and $I_2$ are only depending on the current changed of $I_{D2A}$ and $I_{D2B}$ while $I_1$ is constant. So, the differential output can cancelled identical terms. The linear output current is controlled by controlling voltage ($V_C$) that can be express as

$$I_O = \mu_N C_{ox} \left( \frac{W}{L} \right) \left( V_C - \frac{I_1}{\sqrt{k_n}} - V_{TN} \right) \quad (7)$$

**IV. LOW-SUPPLY FOUR-QUADRANT ANALOG MULTIPLIER**

The drain voltage $V_{DS}$ of $M_{2A}$ and $M_{2B}$ are equalled, which are controlled by $V_C$. The $M_{1A}$ and $M_{1B}$ used for shift-up the input voltage for gate voltage of $M_2$ according to the ohmic condition. The output current is mirrored from $M_{4A}$, $M_{4B}$ by $M_{5A}$, $M_{5B}$. The current $I_1$ and $I_2$ are only depending on the current changed of $I_{D2A}$ and $I_{D2B}$ while $I_1$ is constant. So, the differential output can cancelled identical terms. The linear output current is controlled by controlling voltage ($V_C$) that can be express as

$$I_O = \mu_N C_{ox} \left( \frac{W}{L} \right) \left( V_C - \frac{I_1}{\sqrt{k_n}} - V_{TN} \right) \quad (7)$$

$$I_{D1} - I_{D2} = \mu C_{ox} \left( \frac{W}{L} \right) V_{m} V_{DS} \quad (6)$$

The drain voltage $V_{DS}$ of $M_{2A}$ and $M_{2B}$ are equalled, which are controlled by $V_C$. The $M_{1A}$ and $M_{1B}$ used for shift-up the input voltage for gate voltage of $M_2$ according to the ohmic condition. The output current is mirrored from $M_{4A}$, $M_{4B}$ by $M_{5A}$, $M_{5B}$. The current $I_1$ and $I_2$ are only depending on the current changed of $I_{D2A}$ and $I_{D2B}$ while $I_1$ is constant. So, the differential output can cancelled identical terms. The linear output current is controlled by controlling voltage ($V_C$) that can be express as

$$I_O = \mu_N C_{ox} \left( \frac{W}{L} \right) \left( V_{m} V_{x} V_{y} \right) \quad (8)$$
V. THE SIMULATION RESULTS

The proposed multiplier in Fig. 5 can be confirmed the performances by PSpice. The level 3 model T14Y MOSIS 0.25µm with the $V_{TN} = 0.42 \text{ V}$, $V_{TP} = -0.55 \text{ V}$, $\mu_{N} C_{OX} = 250.1048 \mu A/V^2$ and $\mu_{P} C_{OX} = 51.94153. \mu A/V^2$. The aspect ratio of transistors is shown in Table 1.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L(µm/µm)</th>
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<tr>
<td>M1, M2, M4</td>
<td>1/1</td>
</tr>
<tr>
<td>M3</td>
<td>2/1</td>
</tr>
<tr>
<td>M5</td>
<td>30/1</td>
</tr>
<tr>
<td>M6</td>
<td>20/1</td>
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</table>

Table 1. The aspect ratio of transistors

The DC-characteristic is shown in Fig. 6(a) and (b) while $V_X$ and $V_Y$ input, respectively. It can be shown the linearity and ±400mV dynamic range operation. The linearity error of proposed circuit can be done by fixed maximum input $V_X$ while $V_Y$ is varied and vice versa. The result of linearity error is shown in Fig. 7 that less than 0.5%.

![Fig. 6 The DC-characteristic of proposed multiplier](a)

Fig. 7 Linearity error of proposed multiplier

![Fig. 8](b)

Fig. 8 shows the total harmonic distortion (THD) of proposed circuit can be done by applied $V_X$ at 1MHz with varied amplitude between 0.1-0.8Vp-p. The THD is less than 0.25% within $V_Y$ is different value.
VI. APPLICATION

The other result for the realistic application of proposed circuit is amplitude modulation (AM). The frequency of carrier and input are 10MHz and 500kHz, respectively. The amplitude of both inputs are 0.8Vp-p. The input signal and AM output are shown in Fig. 9.

Fig. 9 The AM output signal while input is 10MHz and 500kHz

VII. Conclusion

This paper proposes a low-voltage, low-distortion four-quadrant analog multiplier. It based on the ohmic transcondance elements and particular sub-circuits. The THD and linearity error are less than 0.25% and 0.5%, respectively. The achieved dynamic range is ±400mV with a single +1.5V power supply condition. The wide bandwidth 34MHz is presented. The good performances are compared with the previous papers. The AM is an application for confirm the realistic applied of proposed circuit.

Table 2 The comparison of proposed circuit with previous works

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<tr>
<td>THD (%)</td>
<td>±3V</td>
<td>±1.4V</td>
<td>±1.5V</td>
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<tr>
<td>Linearity Error</td>
<td>0.6 @10kHz</td>
<td>-</td>
<td>1</td>
<td>2</td>
<td>0.2</td>
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<tr>
<td>Input Range</td>
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<td>±0.4V</td>
<td>±0.8V</td>
<td>±0.8V</td>
<td>±0.4V</td>
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<tr>
<td>freq -3dB</td>
<td>17MHz</td>
<td>-</td>
<td>12MHz</td>
<td>3MHz</td>
<td>34MHz</td>
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<tr>
<td>Tech.</td>
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<td>2µm</td>
<td>0.8µm</td>
<td>0.25µm</td>
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REFERENCES