A Compensated Temperature CMOS Voltage-Controlled Grounded Resistance Circuit

Pipat Prommee, Lersak Yuttasukprasert, Montree Somdulyakanok and Kobchai Dejhan

Faculty of Engineering and Research Center for Communication and Information Technology
King Mongkut’s Institute of Technology Ladkrabang, Bangkok 10520, Thailand
Tel: 66-2326-4238, 66-2326-4242, Fax: 66-2326-4554
E-mail: {pipat, kobchai}@telecom.kmitl.ac.th
1 Faculty of Engineering, Siam University, Bangkok 10160, Thailand

ABSTRACT

A CMOS Voltage-Controlled Grounded Resistor (VCGR) using a new approach for non-linearity terms cancellation is proposed. The proposed circuit uses 17 MOS transistors that operate in ohmic region and saturation region. It consists of the voltage attenuator, voltage differential and voltage inverting circuits. These circuits are performed as a voltage dependent source for biasing an ohmic transistor; cancel the non-linearity terms and threshold voltage in order to compensate the temperature effect. The first order high-pass filter with tunable a cut-off frequency is presented as an application. The proposed circuit characteristics are high linearity and temperature compensation. The results have been confirmed by PSPICE.

1. INTRODUCTION

The Voltage-Controlled Grounded Resistance (VCGR) is widely used in any analog signal processing and usually included in several ICs. The applications are provided for telecommunications and electronics as well as filters, oscillators etc. This paper presents a VCGR with a new approach to cancel non-linear terms with temperature compensation. The results are confirmed their performances by PSPICE.

2. PRINCIPLES

The CMOS VCGRs are rapidly presented with different techniques [1-7]. This paper presents a new technique for cancel nonlinearity terms with temperature compensation. The characteristic of proposed VCGR is high-linearity and low-impact from temperature. This proposed CMOS VCGR consists of 16 transistors for a biased circuit and a transistor for a resistance circuit. The biased circuit consists of the sub-circuits as voltage attenuator, voltage differential, and voltage inverting circuits. The rest transistors operate in ohmic region conforming by the biased circuit. The principle of their circuits can be explained below.

2.1. Ohmic Transistor

The operation of ohmic MOS is shown in Fig. 1 and can be described by the drain current in Eq. (1).

\[ I_D = k_N \left( V_{GS} - V_T + \frac{V_{DS}}{2} \right) V_{DS} \]  

(1)

While \((V_{GS} - V_T) > V_{DS}\)

Where \(k_N = \mu N C_{OX} \left( \frac{W}{L} \right)\)

![Ohmic MOS Transistor](image)

Fig.1. Ohmic MOS Transistor

Regard to Fig.1, the source voltage is grounded. In order to operate under ohmic region condition with the linearity, assume the gate voltage is equal to \(V_T = \frac{V_D + V_C + V_{TN}}{2}\). From this technique, the threshold voltage is disappeared that means the temperature effect is also decreased. The drain current can be rewritten in term of resistance as

\[ R_{eq} = \frac{V_D}{I_D} = \frac{2}{k_N V_C} \]  

(2)

The resistance in Eq. (2) is linearly controlled by \(V_C\).

2.2. Voltage-Attenuator Circuit

The voltage-attenuator was proposed in 1987[8] as shown in Fig. 2.
Fig. 2. NMOS Voltage-Attenuator Circuit

From Fig. 2, $M_1$ and $M_2$ are operated in saturation and ohmic region, respectively. The voltage output can be written as

$$V_O = \left[1-\frac{(W/L)_1}{(W/L)_1+(W/L)_2}\right](V_i-V_{TN}+V_{SS})+V_{SS} \quad (3)$$

Suppose the required output voltage is half the input voltage, therefore we set the aspect ratio of $M_1$ and $M_2$ as $(W/L)_1=3(W/L)_2$. The Eq. (3) will be rewritten as;

$$V_O = \frac{V_i-V_{TN}+V_{SS}}{2} \quad (4)$$

2.3. Voltage-Inverter Circuit

The voltage-inverter circuit consists of 2 NMOS or PMOS transistors that operated in saturation region. Both types of inverter are suited for specific input and output. Both output voltages can be described as;

$$V_O = -V_i \quad (5)$$

Fig. 3. Voltage-Inverter circuit

2.5. Voltage-Differential Circuit

The Voltage-Differential circuit is used in this paper for maintain the controlling voltage of proposed circuit. There are 2 types of NMOS and PMOS transistors as described in Fig. 4 (a) and (b), respectively. The output voltage of N-type can be realized on as;

$$V_O = V_A-V_B + V_{DD} \quad (6a)$$

Likewise, the output voltage of P-type is also realized on

$$V_O = V_A - V_B + V_{DD} \quad (6b)$$

3. VOLTAGE-CONTROLLED GROUNDED RESISTANCE

The VCGR can be implemented using the principle of their particular sub-circuits above. The completed circuit is used 12 NMOS, 4 PMOS transistors and a NMOS for the resistance transistor. The proposed circuit is shown in Fig. 5.

Regard to Fig. 5, the transistor $M_1$ is biased for ohmic operation. The bias voltage is acquired from the different sub-circuits that contains with attenuator, differential, inverter. The input voltage ($V_{in}$) is applied to $M_2$ and $M_3$ that performed as an inverter. The inverter output is applied to the attenuator by $M_4$ and $M_5$. The controlling voltage ($V_C$) is applied to the differential circuit for maintaining the properly voltage by $M_{14}$ and $M_{15}$. The output voltage is inverted by $M_{10}$ and $M_{11}$. The controlling voltage ($V_C$) is applied to the differential circuit for maintaining the properly voltage by $M_{10}$ and $M_{11}$. The output voltage is applied to the inverter $M_{14}$ and $M_{15}$ and passed its output voltage to the attenuator $M_{12}$ and $M_{13}$. The output voltage is inverted by $M_{10}$ and $M_{11}$.

Using the differential circuit $M_6$ and $M_7$ employed output of $M_4$, $M_5$ and output of $M_{10}$, $M_{11}$. The output is adjusted the level by $M_8$ and $M_9$ for bias to gate of $M_1$. The gate voltage of $M_1$ can be realized on

$$V_{G1} = \frac{V_C + V_D}{2} + \frac{V_{DD}}{2} - V_{TN} - V_{B2} \quad (7)$$

Suppose and set the biasing voltage $V_{B1}=-2.5V$ and $V_{B2}=3V$ and $V_{DD}=5V$, the gate voltage in Eq. (7) becomes as;

$$V_{G1} = \frac{V_C + V_D}{2} + \frac{V_{TN}}{2} + 0.75 \quad (8)$$
Consider Eq. (8) and Eq. (1) that can be realized the resistance with the linearity and controllable without temperature effect in term of the threshold voltage as Eq. (9).

\[
R_{eq} = \frac{V_{in}}{I_{in}} = \frac{2}{k_N(V_C + 1.5)}
\]  \hspace{1cm} (9)

4. TEMPERATURE PERFORMANCE

Although the temperature effect in term of the threshold voltage is cancelled. There is another temperature effect in term of surface mobility \(\mu\) that is dominant parameter of the proposed resistance [9]. The temperature effect in this parameter cannot directly be cancelled. The effect can be cancelled by interconnected with the operational transconductance amplifier (V-I) which it has the temperature effect in the same term of surface mobility [9]. The parameter \(\mu\) can be described in Eq. (10) as

\[
\mu(T) = \mu(T_r) \left(\frac{T}{T_r}\right)^{-k_3}
\]  \hspace{1cm} (10)

Where \(T\) is absolute temperature, \(T_r\) is room temperature (Kelvin degree), and \(k_3\) is constant between 1.5 to 2 e.g. the room temperature is varied around 10 degree while \(k_3\) is 1.5, the drain current would be varied about 4.79 to 6.34%.

5. SIMULATION RESULTS

The results of proposed circuit have been confirmed by PSPICE using level 2 ES2 model with the ± 5 volts power supply. The assuming aspect ratio, biasing conditions are the following: (W/L) for \(M_1\) is \((10\mu m/10\mu m)\) the rest transistors are \((50\mu m/10\mu m)\) except the attenuators \(M_4, M_5\) and \(M_{12}, M_{13}\) are using \((75\mu m/10\mu m)\) and \((25\mu m/10\mu m)\), respectively. The DC-Characteristic of proposed circuit is shown in Fig. 6 and the temperature effect result is shown in Fig. 7.

6. APPLICATIONS

The analog signal processing circuits can be applied by using the proposed VCGR. The voltage controlled the first order high-pass filter (HPF) has been used to confirm the application. The configuration of HPF is shown in Fig.8; its frequency response is shown in Fig. 9.

7. CONCLUSION

This proposed VCGR uses the new approach for canceling the non-linearity terms and the temperature effect reduction in term of threshold voltage. However, the temperature effect is still contaminated in term of surface mobility. The temperature effect of surface mobility could be eliminated by interconnect with the operational...
transconductance amplifier (V-I) which also has the temperature effect in the same term of surface mobility [9]. The simulation results by PSPICE have confirmed the high linearity and low-effect of the temperature. The application, voltage controlled HPF is also provided to confirm for the realistic application.

8. REFERENCES


